# Monolithic Integration of CMOS Charge Pumps for High Voltage Generation beyond 100 V

**Monolithische Integration von CMOS Ladungspumpen für Hochvolt-Generierung über 100 V**

Zur Erlangung des akademischen Grades Doktor-Ingenieur (Dr.-Ing.)
genehmigte Dissertation von Dipl.-Ing. Lufei Shen aus Shanghai(CN)
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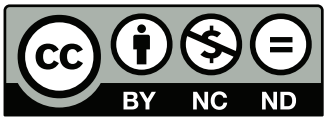

# Erklärung zur Dissertation

Hiermit versichere ich, die vorliegende Dissertation ohne Hilfe Dritter nur mit den angegebenen Quellen und Hilfsmitteln angefertigt zu haben. Alle Stellen, die aus Quellen entnommen wurden, sind als solche kenntlich gemacht. Diese Arbeit hat in gleicher oder ähnlicher Form noch keiner Prüfungsbehörde vorgelegen.

Darmstadt, den 3. July 2014

_____

(Lufei Shen)

# Acknowledgement

The writing of this dissertation is a surprise in my life. As I began to study electrical engineering in 2001, I hadn't dreamed that one day I would be able to do something in microelectronics. The decision between business, economics and engineering was always difficult. The mysteries of electrical engineering seemed however more attractive for a nineteen-years-old boy. Many years are gone, I finally understand that it could be so much fun to deal with technical challenges and to turn own ideas into realities. The procedures can be tough, but the results are enjoyable.

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Darmstadt, 2014

# Kurzfassung

Eine der größten Herausforderungen in Hochspannungs-CMOS SoCs war die monolithische Integration von Aufwärts-Gleichspannungswandlern. Im Vergleich zu einem Aufwärtswandler (engl. boost converter) werden Ladungspumpen als eine vielversprechende Lösung hinsichtlich des Integrationsgrades angesehen. Konventionelle Ladungspumpenarchitekturen zeigen bei der Verwendung als On-Chip-Hochvoltgeneratoren meistens jedoch deutliche Nachteile und Zuverlässigkeitsprobleme auf. Daher werden innovative Ladungspumpenarchitekturen benötigt um die Integration von Ladungspumpen in Hochvoltanwendungen zu realisieren.

In dieser Dissertation werden drei 4-Phasen-Ladungspumpenarchitekturen vorgestellt, welche die dynamische Bulk-Regulierungstechnik und Taktschemen mit Totzeit-Methoden verwenden. Damit werden die Nachteile des Bodyeffektes und das Problem des Rückwärtsstromes in traditionellen Pelliconi-Ladungspumpen bewältigt. Der Einfluss der CMOS Hochvolt-Sandwich-Kondensatoren auf die Spannungsverstärkung und die Energieeffizienz wurden ausführlich untersucht. Die angemessenste Ladungspumpe mit passender Konfiguration der Hochvolt-Sandwich-Kondensatoren wurde gewählt, um zwei Hochvolt-ASICs in einem fortschrittlichen 0,35 $\mu m$ Hochvolt-CMOS-Prozess mit bis zu 120 $V$ zu implementieren. Mit dem ersten Testchip können Spannungen von 120 $V$ aus einer 3,7 $V$ Gleichspannungsquelle erzeugt werden. Damit zeigt er die höchste Ausgangsspannung unter allen veröffentlichten, vollintegrierten CMOS-Ladungspumpen. Messergebnisse bestätigten die Vorteile der vorgeschlagenen Ladungspumpe und den Taktschemen. Der zweite Chip erzeugt eine ähnliche Ausgangsspannung bei deutlich reduzierter Chipfläche. Diese Verbesserung konnte hauptsächlich durch die Verkleinerung der von den Kapazitäten belegte Fläche erreicht werden, was eine Folge der Erhöhung der Taktfrequenz ist. Der zweite Chip arbeitet durch den On-Chip-Taktgenerator außerdem unabhängig von externen Taktsignalen, wodurch die Machbarkeit von integrierten Ladungspumpen für Hochvolt-SoCs gezeigt wird. Basierend auf der erfolgreichen Implementierung dieser zwei Hochvolt-ASICs wurden weitere Betrachtungen der CMOS-Ladungspumpen mit Hilfe von Simulations- oder Messergebnissen durchgeführt. Diese beinhalten die Stabilität der Ausgangsspannung, den Integrationsgrad sowie die Limitierungen bei der Erzeugung von negativen Hochvoltspannungen. Eine Regulierung der Rückkopplung durch Anpassung der Taktfrequenz oder der Gleichspannungsversorgung ermöglicht eine effektive Stabilisierung der Ausgangsspannung. Diese Rückkopplung kann leicht auf dem Chip integriert werden. Durch eine Erhöhung der Taktfrequenz kann eine erhebliche Reduzierung der Kapazität erreicht werden, was zu einer Verkleinerung der benötigten Chipfläche führt. Ein Anwendungsbeispiel zeigt die Wichtigkeit von vollintegrierten Hochvolt-Ladungspumpen.

Außerdem wird eine neue Entwicklungsmethode für die On-Chip-Hochvoltgenerierung in CMOS-Technologien vorgeschlagen. Sie beinhaltet Konstruktionsverfahren für On-Chip Aufwärts-Gleichspannungswandler sowie einen allgemeinen Designflow, der sich hauptsächlich auf die Machbarkeit und die Zuverlässigkeit von Hochspannungs-CMOS-ASICs konzentriert.

In dieser Dissertation wurde bestätigt, dass CMOS-Ladungspumpen mit passenden Architekturen, die sowohl die benötigte Chipfläche als auch die Zuverlässigkeit der Schaltung berücksichtigen, für die On-Chip-Hochvoltgenerierung bei Spannungen über 100 $V$ eingesetzt werden können. Einige Verbesserungsmöglichkeiten zur Steigerung der Leistungsfähigkeit der Schaltung und zur Erweiterung der Funktionalität von Hochvoltladungspumpen werden für weiterführende Arbeiten vorgeschlagen.

# Abstract

Monolithic integration of step-up DC-DC converters used to be one of the largest challenges in high voltage CMOS SoCs. Charge pumps are considered as the most promising solution regarding integration levels compared to boost converter with bulky inductors. However, conventional charge pump architectures usually show significant drawbacks and reliability problems, when used as on-chip high voltage generators. Hence, innovative charge pump architectures are required to realize the monolithic integration of charge pumps in high voltage applications.

In this dissertation, three 4-phase charge pump architectures with the dynamic body biasing technique and clock schemes with dead time techniques were proposed to overcome drawbacks such as body effect and reverse current problem of traditional Pelliconi charge pump. The influences of high voltage CMOS sandwich capacitors on the voltage gain and power efficiency of charge pumps were extensively investigated. The most reasonable 4-phase charge pump architecture with a suitable configuration of high voltage sandwich capacitors regarding the voltage gain and power efficiency was chosen to implement two high voltage ASICs in an advanced $120\,V$ $0.35\,\mu m$ high voltage CMOS technology. The first test chip operates successfully and is able to generate up to $120\,V$ from a $3.7\,V$ low voltage DC supply, which shows the highest output voltage among all the reported fully integrated CMOS charge pumps. The measurement results confirmed the benefits of the proposed charge pump architectures and clock schemes. The second chip providing a similar output voltage has a reduced chip size mainly due to decreased capacitor areas by increased clock frequencies. Furthermore, the second chip with an on-chip clock generator works independently of external clock signals which shows the feasibility of integrated charge pumps as part of high voltage SoCs. Based on the successful implementation of those high voltage CMOS ASICs, further discussions on the stability of the output voltage, levels of integration and limitations in the negative high voltage generation of high voltage CMOS charge pumps are held with the aid of simulation or measurement results. Feedback regulation by adjusting the clock frequency or DC power supply is able to stabilize the voltage performance effectively while being easily integrated on-chip. Increasing the clock frequency can significantly reduce the required capacitor values which results in reduced chip sizes. An application example demonstrates the importance of fully integrated high voltage charge pumps.

Besides, a new design methodology for the on-chip high voltage generation using CMOS technologies was proposed. It contains a general design flow focusing mainly on the feasibility and reliability of high voltage CMOS ASICs and design techniques for on-chip high voltage generators.

In this dissertation, it is proven that CMOS charge pumps using suitable architectures regarding the required chip size and circuit reliability are able to be used as on-chip high voltage generators for voltages beyond $100\,V$. Several methods to improve the circuit performance and to extend the functionalities of high voltage charge pumps are suggested for future works.

# Contents

# Abbreviations

2D Two-Dimensional

3D Three-Dimensional

ASIC Application-Specific Integrated Circuit

BCD Bipolar-CMOS-DMOS

BJT Bipolar Junction Transistor

BOX Buried Oxide

BSIM Berkeley Short-channel IGFET Model

BST Barium-Strontium-Titanate

CMOS Complementary Metal-Oxide-Semiconductor

Cocoon Cooperative sensor communication

D/A Digital/Analog

DC Direct Current

DRC Design Rule Check

DTI Deep Trench Isolation

EDA Electronic Design Automation

ERC Electrical Rule Check

ESD Electrostatic Discharge

ESR Equivalent Series Resistance

FOX Field Oxide

GDSII Graphical Design Station II

GPS Global Positioning System

HCI Hot Carrier Injection

HiSIM Hiroshima-university STARC IGFET Model

HVMOS High Voltage MOS

I/O Input/Output

IC Integrated Circuit

IP Intellectual Property

JFET Junction FET

LDMOS Laterally Diffused MOS

LOEWE Landes-Offensive zur Entwicklung Wissenschaftlich-ökonomischer Exzellenz

Ltacc Life time acceleration factor

LVS Layout versus Schematic

MEMS Micro-Electro-Mechanical System

MIM Metal-Insulator-Metal

MM20 MOS Model 20

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

NBTI Negative-Bias Temperature Instability

NMOS N-type Metal-Oxide-Semiconductor

PCB Printed Circuit Board

PCell Parameterized Cell

PDK Process Design Kit

PFM Pulse Frequency Modulation

PMOS P-type Metal-Oxide-Semiconductor

PVT Process, Voltage, Temperature

PWM Pulse Width Modulation

RESURF Reduced Surface Field

RF Radio Frequency

SEPIC Single Ended Primary Inductance Converter

SiP Sytem-in-Package

SMD Surface Mounted Device

SOA Safe Operating Area

SOAC Safe Operating Area Check

SoC System-on-Chip

SOI Silicon-on-Insulator

SPICE Simulation Program with Integrated Circuit Emphasis

STI Shallow Trench Isolation

TDDB Time Dependent Dielectric Breakdown

TMN Tunable Matching Network

TSV Through Silicon Vias

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# 1 Introduction

The miniaturization of semiconductor devices according to Moore's Law [A51] has reached the technology node of 14 $nm$ in 2014 [Che14]. This transistor scaling is mostly intended to realize digital functionalities and it will come to an end in the near future [Hru13]. However, it is not necessary to scale down devices at the same rate to allow more non-digital functionalities on-chip. Moreover, non-digital devices can not be shrunk like digital ones due to their physical limitations such as breakdown voltages, saturation currents, linearity etc. In order to integrate more functionalities to semiconductor products, More-than-Moore [Ae10] becomes a new trend. Microelectronic advancements achieved by More-than-Moore cover a wide range of fields, for instance, MEMS (Micro-Electro-Mechanical System) applications including sensors and actuators, RF (Radio Frequency) applications such as Bluetooth and GPS (Global Positioning System), and high voltage applications requiring high voltage amplifiers and high voltage generators. Especially on-chip high voltage generators using mostly step-up DC-DC (Direct Current) converters, are gaining more and more importance in battery-powered mobile applications. The generated high voltages are used to power circuit blocks enabling various non-digital functionalities.

## 1.1 Motivation

CMOS (Complementary Metal-Oxide-Semiconductor) technology is recognized as the mainstream technology in the semiconductor industry. Their applications were usually limited to low voltage domains (below 5 $V$) due to their technological constraints like low breakdown voltages. Hence, high voltage applications were dominated by BCD (Bipolar-CMOS-DMOS) and SOI (Silicon-on-Insulator) technologies in the past. With the rapid development of CMOS technologies, high voltage CMOS technologies exhibiting BCD-like performance and compatible with standard CMOS processes are proven to be reliable and cost-effective [BRN09; Sch+08; Min11; Par08; PS11]. The minimum feature sizes of high voltage CMOS technologies have decreased from 0.8 $\mu m$ through 0.35 $\mu m$ to 0.18 $\mu m$ with improved maximum operating voltages of up to 120 $V$ [Dat14c; Dat14b; Dat14g; Dat14d; Dat14f; MK10]. Figure 1.1 illustrates the increasing miniaturization of high voltage CMOS ASICs (Application-Specific Integrated Circuit). Using technologies with smaller feature sizes but the same maximum operating voltages, required functionalities can be implemented with more compact chip sizes.

Under this background, it is expected that step-up DC-DC converters such as charge pumps and boost converter can be fully integrated in CMOS technologies to realize the on-chip high voltage generation. Many applications such as MEMS [Zl07], energy harvester [CT12], reconfigurable antenna array [NH13] etc. require these on-chip high voltage generators, particularly in portable devices, where only low voltage batteries are available. A high level of integration is desirable to realize high voltage SoCs (System-on-Chip) with optimized chip sizes, reduced production costs as well as improved performance and reliability. Figure 1.2 illustrates a monolithic solution of a complex high voltage SoC, wherein high voltage and low voltage circuit parts are powered by the on-chip high voltage generator and low voltage regulator, respectively.

Since the shrinking of high voltage CMOS technologies needs to overcome more complicated physical effects such as HCI (Hot Carrier Injection), TDDB (Time Dependent Dielectric Breakdown), NBTI (Negative-Bias Temperature Instability) etc. [See11], high voltage CMOS technologies with the highest maximum operating voltages, typically 120 $V$, remain at the technology node of 0.35 $\mu m$. This implies that higher integration levels of on-chip high voltage generators can mostly be reached

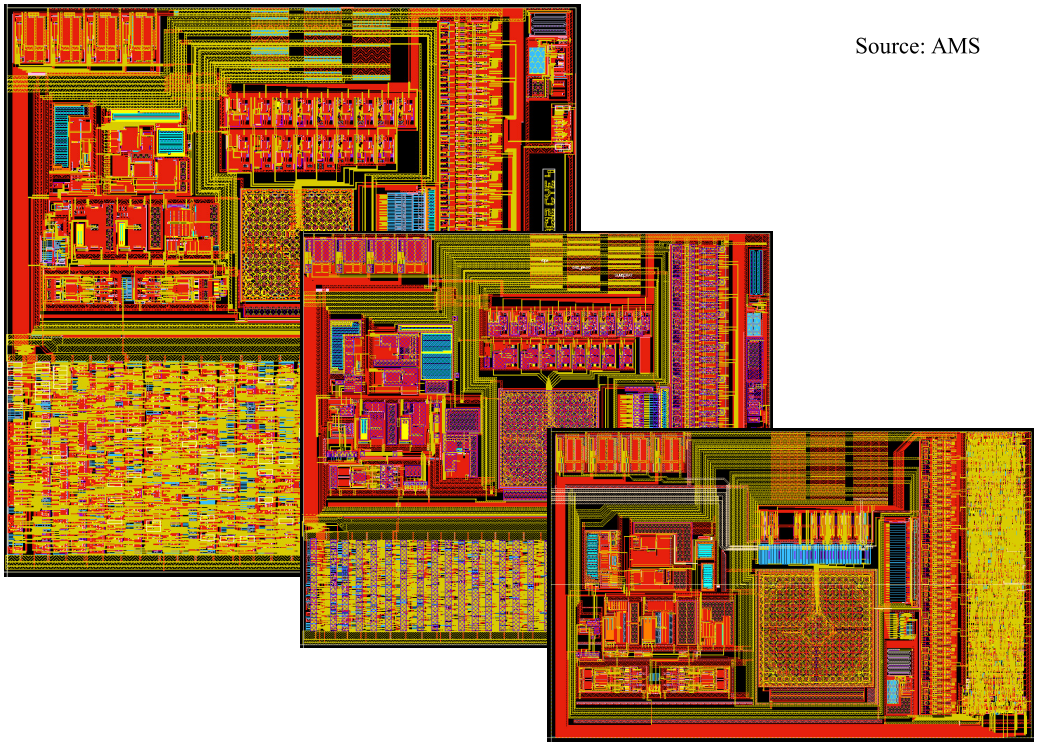



**Figure 1.1.:** Increasing miniaturization of high voltage CMOS ASICs.

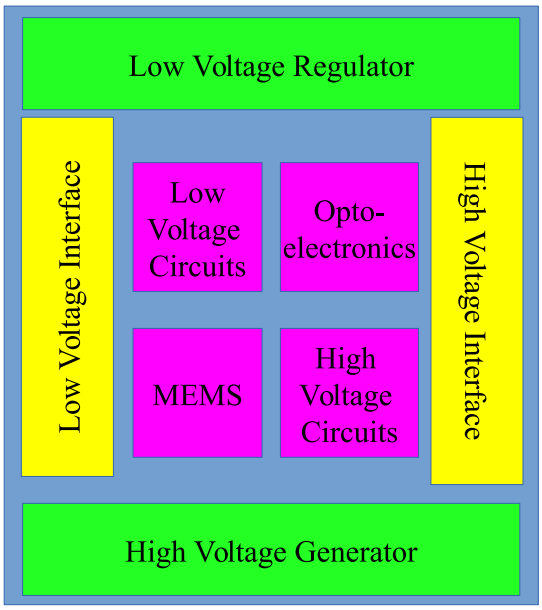



**Figure 1.2.:** A typical high voltage SoC.

by employing more advanced circuit architectures. Charge pumps composed of only switches and capacitors can easily be monolithically integrated compared to boost converter with large inductors. However, many conventional charge pump architectures are not suitable for high voltage applications due to their reliability problems. Furthermore, step-up charge pump architectures such as Dickson charge pump [Dic76] and Pelliconi charge pump [PR03] can be applied but show their significant drawbacks, which lead to very low voltage gain and consequently extremely large layout area. Therefore, innovative charge pump architectures to realize on-chip high voltage generation with reasonable chip sizes are of great interest.

## 1.2 State of the Art

Step-up DC-DC conversion is currently accomplished by partially integrated boost converters with discrete components such as inductors, diodes and capacitors. This results in large footprints on PCBs (Printed Circuit Board). The main reason is that the required high inductance values can only be obtained by using external inductors. Moreover, on-chip inductors of small inductance occupy large layout areas and have high ESR (Equivalent Series Resistance) [SN13; SW11; HG10; KK13; VPA13]. Therefore, the low-quality but large-sized on-chip inductors are the major obstacle for the monolithic integration of boost converter.

Dickson charge pump has been employed and implemented in SOI technologies to generate high output voltages up to $70\,V$ [BS09]. However, the body diodes of the MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistor) are used as switches in this on-chip high voltage Dickson charge pump. The main problems of Dickson charge pump such as the body effect problem and low voltage gain remain unsolved. Besides, in both CMOS and SOI technologies, body diodes are usually parasitic diodes and not suggested to be used as standard devices [Dat14c; Dat14b; Dat14g; Dat14f]. The reliability of circuits using body diodes is a potential problem.

In CMOS technologies, most charge pump architectures are adopted to realize low voltage conversion, where no high voltage conversion ratios are necessary. For example, to generate a $120\,V$ output voltage from a low voltage DC supply of $3.7\,V$, which means a voltage conversion ratio higher than 32, high voltage gain resulting in decreased stage number is required to reduce the final chip size. Considering the high voltage stress of up to $120\,V$, the reliability of devices in the circuit challenges many charge pump architectures. Therefore, the main discussion on fully integrated high voltage CMOS charge pumps stays at the simulation levels. Effective and reliable charge pump architectures have still not been published. The reported charge pump with the highest output voltage of $55\,V$ from a $3\,V$ low voltage supply in CMOS technologies is based on Dickson charge pump using the body diodes of MOSFETs [Dou10].

## 1.3 Objectives

The main task of this dissertation is to study the possibility to integrate charge pumps using CMOS technologies for the on-chip high voltage generation. $120\,V$ is chosen as the final output voltage, since the current high voltage CMOS technologies operate at a maximum of $120\,V$. $3.7\,V$ is chosen as the initial input voltage, because it represents the typical battery voltages in portable devices.

Due to the required high voltage conversion ratio, innovative charge pump circuit architectures for the optimization of voltage gain, power efficiency, reliability etc. are indispensable to overcome the drawbacks of conventional charge pump architectures. The chosen architecture is supposed to be implemented and verified in the form of high voltage ASICs, which are intended to prove the monolithic integration of high voltage charge pumps with reasonable chip sizes. Furthermore, approaches to increase the integration level and to improve the voltage performance have to be investigated in order to demonstrate the possible miniaturization and optimization of fully integrated high voltage charge pumps.

## 1.4 Thesis Outline

This dissertation is split into the following chapters:

- **Chapter 1** introduces the development of high voltage CMOS technologies and the necessity of monolithically integrated high voltage generators. State of the art of step-up DC-DC converters such as boost converter and charge pumps for the on-chip high voltage generation is presented. The objectives of this dissertation are also clarified and defined.
- **Chapter 2** contains discussions on the principles of boost converter and charge pumps. High voltage CMOS technologies are introduced in detail. A comparison regarding the integration level of integrated boost converter and charge pumps is given, which concludes that charge pumps are more suitable to realize monolithic step-up DC-DC converters in CMOS technologies.
- **Chapter 3** describes a new design methodology for the on-chip high voltage generation using CMOS technologies. Special characteristics of device models in design kits for high voltage CMOS technologies are explained. Moreover, a general design flow focusing mainly on the feasibility and reliability of high voltage CMOS ASICs is proposed. An extensive discussion about design techniques for on-chip high voltage generators helps designers optimizing related design techniques.
- **Chapter 4** presents proposed charge pump architectures for the monolithic integration in comparison to conventional charge pumps. Combined with advanced 4-phase clock schemes with dead time techniques, these proposed architectures show significantly improved voltage performance and sufficient reliability against high voltage stresses. One of the proposed architectures was selected for the implementation in a typical high voltage CMOS technology. The first test chip operates successfully and is able to generate up to $120\,V$ from a $3.7\,V$ low voltage DC supply. The measurement results confirm the benefits of the proposed charge pump architectures and clock schemes. The second chip, providing similar voltage performance, has a reduced chip size mainly due to the decreased capacitor areas at the increased clock frequency. Furthermore, with the on-chip clock generator, the second chip works independently of external clock signals, which proves the possibility to integrate charge pumps as a part of high voltage SoCs. Based on the successful implementation of two high voltage CMOS ASICs, further discussions on the stability, levels of integration and limitations of high voltage CMOS charge pumps are conducted by simulation or measurement results. At last, an application example is given to demonstrate the importance of fully integrated high voltage charge pumps.
- **Chapter 5** summarizes the whole dissertation and concludes that charge pumps using CMOS technologies can be adopted as on-chip high voltage generators for voltages beyond $100\,V$. However, suitable circuit architectures must be chosen to provide a reasonable chip size and adequate circuit reliability. Finally, several methods to improve the circuit performance and to extend the functionalities of high voltage charge pumps are suggested.

# 2 On-chip High Voltage Generation with CMOS Technologies

The voltage level for high voltages in CMOS technologies is not explicitly defined. Commonly, operating voltages above 5 $V$ are already considered as high voltages. However, the generation of high voltages up to 120 $V$ from low battery voltages such as 3.7 $V$ by means of current CMOS technologies is still very challenging, since it requires special circuit architectures and design techniques. The limited choice of available devices in CMOS technologies increases also the difficulty to realize circuit architectures, which are already proven in the form of discrete circuits. The level of integration of high voltage generators affects directly the number of necessary components and the size of PCBs. High integration level will significantly reduce the production costs. Besides, there is another benefit of high level of integration in energy efficiency by saving I/O (Input/Output) power. Therefore, it is of great importance to choose a circuit architecture with high level of integration for the on-chip high voltage generation. Since most reported researches in literatures such as [SN13; SW11; VPA13] discuss only DC-DC converters in low voltage domains, a comprehensive study regarding the integration level of high voltage DC-DC converters is becoming in great demand.

## 2.1 DC-DC Converters

A DC-DC converter is a circuit architecture, which transforms input voltages into higher, lower or even inverted output voltages. There are many circuit topologies of DC-DC converters, such as boost converter, charge pumps, buck converter, buck-boost converter and so on. For the high voltage generation from low voltage batteries by CMOS technologies, we focus on boost converter and charge pumps, which are able to increase the voltage level of input voltages. Due to the restrictions of portable battery-powered devices, applications of low power consumption are mainly concerned.

### 2.1.1 Boost Converter

When available low voltage power supplies are no more sufficient, boost converter is frequently adopted to generate required high voltage power supplies. In Figure 2.1, the principle circuit diagram of boost converter with ideal components is illustrated. The transistor $M_1$ operates as a switch, which is typically controlled by the pulse-modulated clock signal $V_{ctrl}$. By means of an energy storage element, namely the inductor $L_1$, electrical energies will be transformed in magnetic energies and stored during the switch-on state of the switch $M_1$. When the switch $M_1$ is switched off, such magnetic energies will be transformed back to electrical energies again and transferred to the output capacitor $C_1$. After the voltage level at the output is higher than that at the anode of the diode $D_1$, the diode $D_1$ will be turned off, so that the normal operation of boost converter can be ensured.

There exist two operation modes of boost converter, the discontinuous mode and continuous mode, which depend on whether the inductor current decreases to zero during the switch-off state of the switch $M_1$ [WS11]. Normally, the continuous mode is preferred for the implementation, since the voltage gain between $V_{out}$ and $V_{in}$ is merely determined by the duty cycle $k$ of the pulse-modulated clock signal $V_{ctrl}$.

The general circuit analysis on the continuous mode of boost converter can be explained in the following way [WS11; PM09]:

The inductor $L_1$ is charged up, when the switch $M_1$ is closed. This switch-on duration is represented by $T_{on} = kT_{period}$.

$$L\frac{\mathrm{d}i_{in}}{\mathrm{d}t} = V_{in} = L\frac{\Delta i_{in}}{T_{on}} = L\frac{\Delta i_{in}}{kT_{period}} \tag{2.1}$$

The magnetic energy stored in the inductor $L_1$ and the electrical energy from the input voltage $V_{in}$ are transferred to the output, when the switch $M_1$ is open. That means certain current flows through the inductor $L_1$ and the diode $D_1$ to the load of boost converter, which will reach its maximum output voltage level.

$$L\frac{\mathrm{d}i_{in}}{\mathrm{d}t} = V_{in} - V_{out} = -L\frac{\Delta i_{in}}{T_{off}} = -L\frac{\Delta i_{in}}{(1-k)T_{period}} \tag{2.2}$$

Since the current through the inductor $L_1$ changes only continuously, the $\Delta i_{in}$ during the switch-on and -off state of $M_1$ should be identical.

$$\frac{kT_{period}V_{in}}{L} = (V_{out} - V_{in})\frac{(1-k)T_{period}}{L} \tag{2.3}$$

Finally, we obtain $V_{in} = (1-k)V_{out}$. Figure 2.2 illustrates the timing diagram of the currents in boost converter. The control of the duty cycle $k$ of the clock signal $V_{ctrl}$ can be realized by PWM (Pulse Width Modulation) in order to stabilize the output voltage at certain voltage levels in case of unstable load conditions.

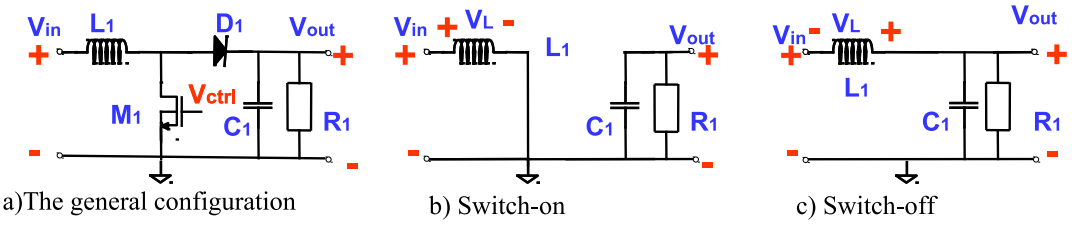



**Figure 2.1.:** Circuit diagram of boost converter.

The diode $D_1$ can be replaced by switching transistors. In those cases, complex control signals with sufficient voltage levels and correct timing are required to ensure the normal operation of boost converter. Other DC-DC converters such as SEPIC (Single Ended Primary Inductance Converter), which also employ inductors as energy transfer elements for the high voltage generation, are introduced in [WS11; PM09; Man05]. These DC-DC converters have however more complicated circuit architectures but provide similar circuit performance compared with boost converter.

### 2.1.2 Charge Pumps

Charge pumps are another type of commonly used DC-DC converters, which can increase input voltages to higher voltage levels adopting only capacitors and switches. In comparison to boost converter, the voltage gain between $V_{out}$ and $V_{in}$ of charge pumps depends mostly on circuit topologies instead of duty cycles of clock signals. By periodically switching of switches, electrical charge stored

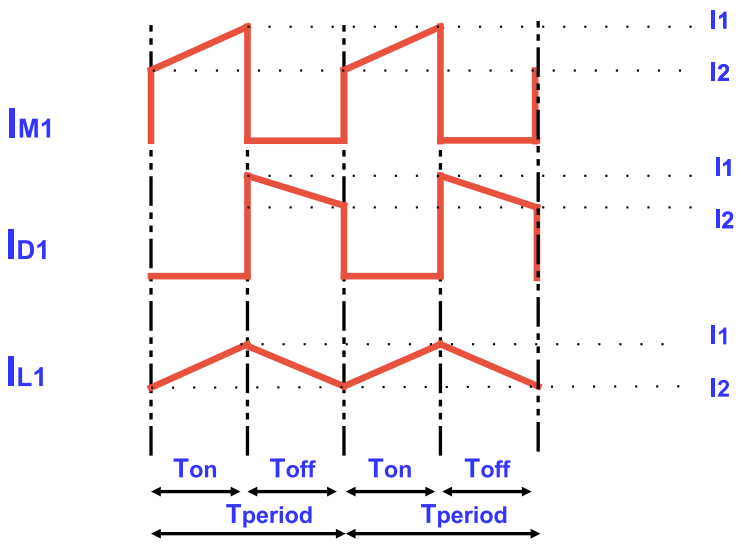
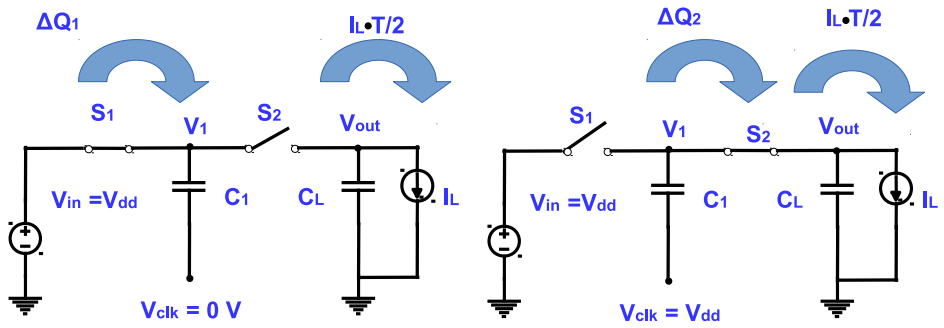



**Figure 2.2.:** Current flows in boost converter.

in pumping capacitors is delivered to the output. The concrete realization of such charge transportation is determined by circuit topologies. Among numerous already published charge pump architectures [BS13; Tan13], Dickson charge pump [Dic76] is very popular in integrated circuits because of its simplicity.

The functional principle of Dickson charge pump is shown in Figure 2.3. For simplification, only a single stage is discussed and all the components are ideal.




a) The first half period

b) The second half period

**Figure 2.3.:** Functional principle of a single stage Dickson charge pump.

When no load current exists, the voltage level at the pumping capacitor $C_1$ will be charged up to $V_{dd}$ by the voltage source $V_{in}$ during the first half period of the clock signal $V_{clk}$. After that, the charge stored in the pumping capacitor $C_1$ will be transferred to the load capacitor $C_L$ during the second half period. In consequence of charge redistribution and charge conservation, the output voltage $V_{out}$ will finally reach $2V_{dd}$ at the final stable state. Such results can also be explained in the following equations, where $V_{out}(j)$ represents the current output voltage and $V_{out}(j-1)$ the former one.

$$(C_1 + C_L)V_{out}(j) = C_1 2V_{dd} + C_L V_{out}(j-1) \tag{2.4}$$

At the final stable state of a single stage Dickson charge pump:

$$V_{out}(j) = V_{out}(j-1) = V_{out}(\text{steady}) = 2V_{dd} \tag{2.5}$$

Detailed mathematical analysis can be found in [PP10]. It is evident that the input voltage $V_{in}$ of a single stage Dickson charge pump will be ideally increased to $2V_{dd}$.

When the load current $I_L$ is no longer negligible, the 1-stage Dickson charge pump must be able to provide additional charge of $\Delta Q = I_L T$ during each second half period[1]. The rule of charge redistribution and charge conservation are applied here as well.

$$(C_1 + C_L)V_{out}(j) + I_L T = C_1 2V_{dd} + C_L V_{out}(j-1) \tag{2.6}$$

And that results in:

$$V_{out}(j) = V_{out}(j-1) = V_{out}(\text{steady}) = 2V_{dd} - \frac{I_L T}{C_1} \tag{2.7}$$

Multistage Dickson charge pump with ideal components operates in the similar way. For example, a 2-stage Dickson charge pump can be considered as a single-stage Dickson charge pump, which takes the output voltage of the first stage of the original 2-stage Dickson charge pump as its input voltage. For an n-stage Dickson charge pump, the overall voltage gain can be derived as follows:

Without load current $I_L$:

$$V_{out}(\text{steady}) = (n+1)V_{dd} \tag{2.8}$$

With load current $I_L$ and assuming $C_1 = C_2 = \ldots = C_n$:

$$V_{out}(\text{steady})_1 = 2V_{dd} - \frac{I_L T}{C_1}, \text{ when } n = 1. \tag{2.9}$$

$$V_{out}(\text{steady})_2 = 3V_{dd} - 2\frac{I_L T}{C_1} = V_{out}(\text{steady})_1 + V_{dd} - \frac{I_L T}{C_1}, \text{ when } n = 2. \tag{2.10}$$

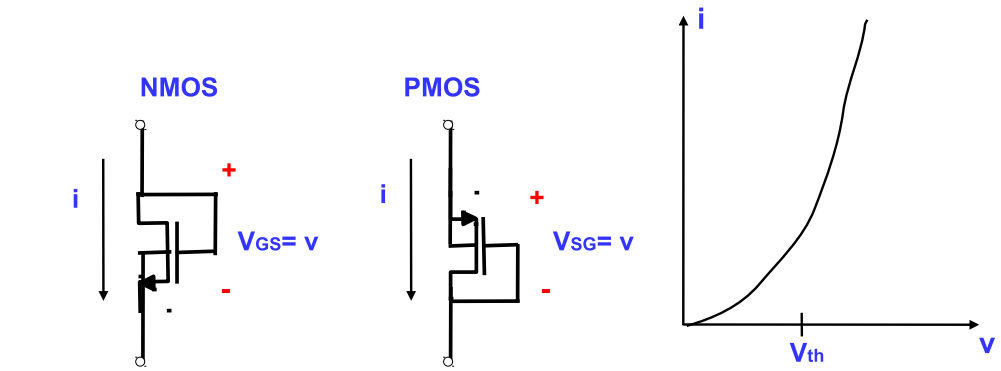
...

$$V_{out}(steady)_n = (n+1)V_{dd} - n\frac{I_L T}{C_1}, \text{ when } n = n. \tag{2.11}$$

The switches in Dickson charge pump are principally realized by diodes. However, the available diodes in current CMOS technologies are usually parasitic diodes, which occupy large chip area but show very poor performance. Therefore, CMOS transistors are employed as the replacement for diodes in CMOS technologies to build integrated Dickson charge pump (see Figure 2.4.) $V_{th}$ is the threshold voltage of CMOS transistors. In ideal cases, $V_{th}$ is assumed to be zero.

A typical n-stage Dickson charge pump is presented in Figure 2.5.

[1] $\frac{\Delta Q}{2} = \frac{I_L T}{2}$ to the load capacitor to compensate the previous voltage drop and $\frac{\Delta Q}{2} = \frac{I_L T}{2}$ directly to the load resistor in the form of the load current $I_L$.




a) Diode-connected NMOS b) Diode-connected PMOS c) I-V curve

**Figure 2.4.:** Diode-connected CMOS transistors.

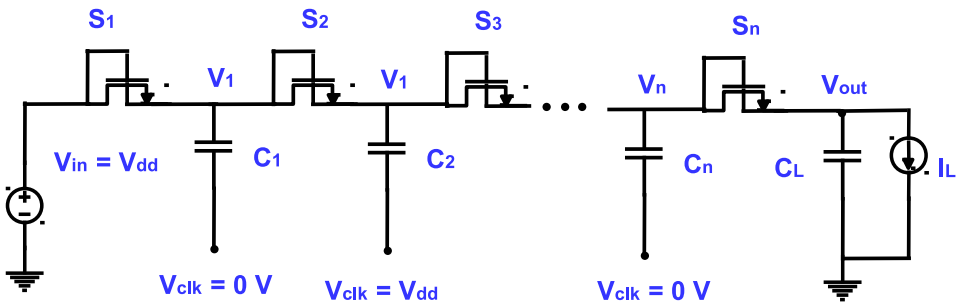



**Figure 2.5.:** Circuit diagram of a multistage Dickson charge pump.

If the threshold voltage $V_{th}$ of CMOS transistors can not be neglected, the output voltage $V_{out}$ is calculated in following [PS06]:

$$V_{out}(steady)_n = (n+1)V_{dd} - n\frac{I_L T}{C_1} - (n+1)V_{th}, \text{ when } n = n. \tag{2.12}$$

Due to the considerable voltage drop over diodes or diode-connected transistors in practice, the stage voltage gain of Dickson charge pump is limited and always much lower than the DC supply voltage $V_{dd}$. To reduce such gain loss, many modified Dickson charge pump architectures such as bootstrap charge pump are proposed [PP10]. These architectures require however doubled clock voltage levels and several additional transistors to achieve the reduction of the voltage drop caused by diodes or diode-connected transistors in Dickson charge pump.

Hence, another type of charge pumps, which is different from Dickson charge pump and easy to be implemented, was proposed by Pelliconi [PR03]. The basic circuit of a single stage Pelliconi charge pump is shown in Figure 2.6. This charge pump architecture uses control signals to switch on and off the MOS switches, while diodes or diode-connected transistors in Dickson charge pump circuits are passively turned on and off by the voltage difference between both device terminals. All the Node $A$ in the circuit are connected together. The same case is also for all the Node $B$. For Pelliconi charge pump, the most important thing is to design control signals always ensuring correct timing and voltage levels for each MOS switch.

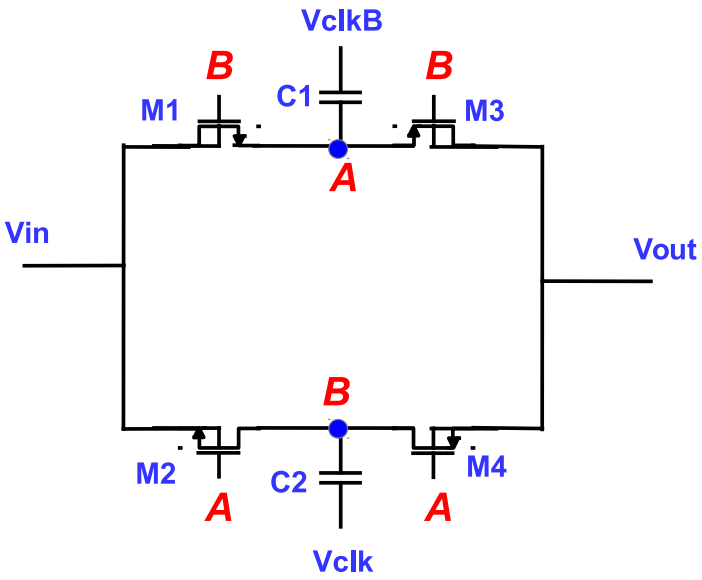



**Figure 2.6.:** Circuit diagram of a single stage Pelliconi charge pump.

The 2-phase non-overlapping clock signals $V_{clk}$ and $V_{clkB}$ operate not only as control signals of the MOS switches but also as the DC power supply, which transfers charge from stage to stage. In this way, voltage levels of the node $A$ and $B$ at the both pumping capacitors $C_1$ and $C_2$ serve as the control signals for the related NMOS and PMOS switches. Because the voltage drop over each switch is not threshold voltage $V_{th}$ of the MOS switches, in comparison to Dickson charge pump circuits with diode-connected transistors, but the usually very low forward conduction voltage drop of the MOS switches, therefore, the stage voltage gain is considerably improved. Furthermore, since the two pumping capacitors $C_1$ and $C_2$ transfer the charge to the load capacitor $C_L$ at each half period of the clock alternatively, the output voltage ripple $\Delta V_{out}$ is much lower than that of Dickson charge pump, in which the charge is only transferred to the load capacitor $C_L$ during each second half clock period. A circuit diagram explaining the charge transfer principle in Pelliconi charge pump is illustrated in

Figure 2.7[2]. The theoretical and experimental comparison between Pelliconi and Dickson charge pump can be found in [BP05], which has proven the advantages of Pelliconi charge pump such as higher voltage gain and power efficiency.

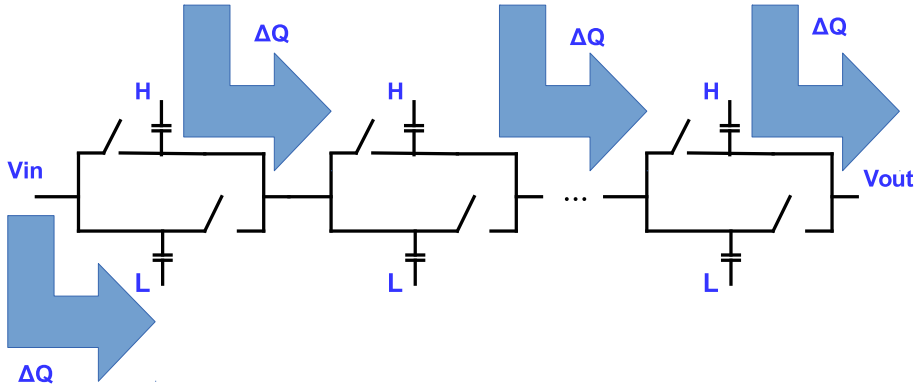



**Figure 2.7.:** Charge transfer principle in an n-stage Pelliconi charge pump.

The mathematical description of the voltage gain at an n-stage Pelliconi charge pump with ideal components is concluded as following [PR03][3]:

$$V_{out} = V_{dd} + n(V_{clk} - \frac{I_L}{2fC}), \text{ where } V_{clk} = V_{dd} \tag{2.13}$$

Other charge pump architectures like heap charge pump, Fibonacci charge pump etc. are discussed in [AG09; ABT05; BS13; Tan13]. These architectures have also the potential to generate high output voltages. However, the most related researches concentrated only on circuit structures instead of concrete implementation of the circuits. This makes it difficult to adopt them directly for the high voltage generation considering the feasibility and reliability.

## 2.2 High Voltage CMOS Technologies

To generate high voltages with CMOS integration requires CMOS technologies with high breakdown voltage $V_{bd}$ and low specific on-resistance $R_{on}$. High $R_{on}$ results in high voltage losses, and low $V_{bd}$ leads to instability of the circuit. Recent developments of advanced high voltage CMOS technologies show that CMOS technologies can provide BCD-like performance but with low process complexity and fabrication costs [Dat14c; Dat14b; Dat14g; Dat14d; MK10].

### 2.2.1 Device Structures

High voltage devices such as transistors and capacitors in present high voltage CMOS technologies have mostly different structures from those in standard CMOS processes. In Figure 2.8, simplified cross sections of common high voltage CMOS transistors are illustrated. The horizontal breakdown voltage between Drain and Source (Gate) terminals of the transistors is increased through the introduction of the drift region by RESURF (Reduced Surface Field) techniques underneath the wide FOX (Field Oxide). Principally, high voltage CMOS transistors belong to LDMOS (Laterally Diffused MOS), which using RESURF techniques to extend lateral breakdown voltages. However, longer drift

[2] $H$ stands for the high voltage level of clock signals, namely $V_{dd}$. $L$ stands for the low voltage level of clock signals, namely 0.

[3] $T$ is the clock period, $f$ is the clock frequency and $C$ is the pumping capacitor.

region and lower doping concentration to achieve higher breakdown voltages result in higher on-resistance of the transistor as well. To reduce the undesirable on-resistance, the channel width of the transistor needs to be increased. For high voltage CMOS transistors with low on-resistance, large layout size is inevitable [Par08; PS11]. In addition to asymmetrical LDMOS devices for unidirectional operations, symmetrical high voltage MOS devices with drift regions at both Source and Drain sides and therefore even larger size are also available to support bidirectional operations, for example, in applications such as transmission gates. The horizontal breakdown voltage between Bulk and Source terminals is still low voltage due to similar structures compared to those in low voltage CMOS processes. Although thicker gate oxide can be adopted to increase the breakdown voltages between Gate and Source terminals, this method is usually effective to achieve high breakdown voltages up to about $20\,V$. At the same time, the threshold voltages of transistors with thicker gate oxide will become higher as well, which is in most cases not desired. The vertical breakdown voltage from each terminal of transistors to the p-substrate reaches the reverse breakdown voltages between the deep NWELL and p-substrate, which is recently reported to be able to withstand up to $120\,V$ in high voltage CMOS technologies [Dat14c].

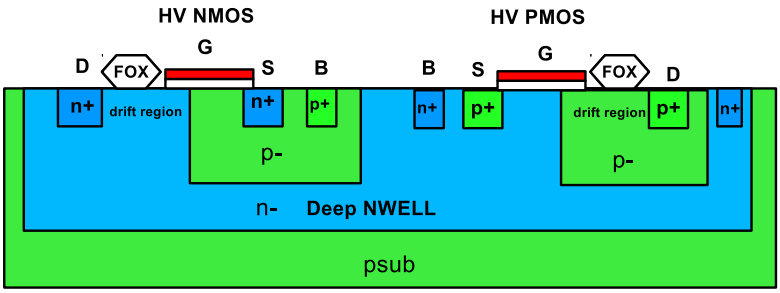
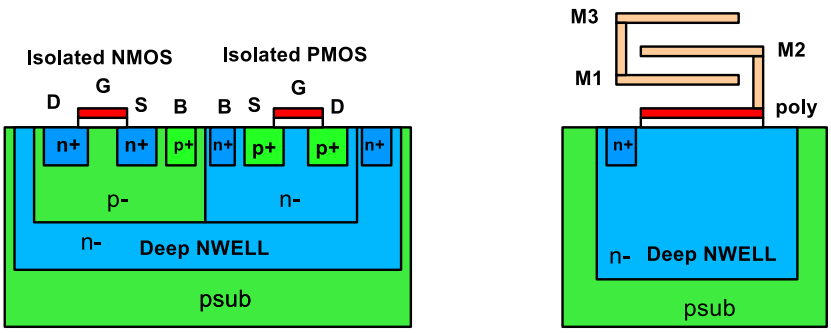



**Figure 2.8.:** Simplified cross sections of high voltage NMOS and PMOS transistors.

In Figure 2.9, other useful devices for high voltage applications are displayed. Isolated low voltage CMOS transistors with deep NWELLs in the p-substrate have the same vertical breakdown characteristics as those high voltage CMOS transistors, but their horizontal breakdown characteristics remain low voltage. The benefits of the introduced deep NWELL to enlarge vertical breakdown voltages can also be found in high voltage sandwich capacitors. Each terminal of such high voltage capacitors can withstand as high as the breakdown voltages between the deep NWELL and p-substrate. On-chip planar inductors such as spiral inductors are usually not standard devices in high voltage CMOS technologies. Even carefully designed by designers, on-chip inductors of only a couple of nanohenry can be achieved with acceptable layout sizes and quality factors in RF applications [MO09; KK13; SW11].

### 2.2.2 Device Features

Due to complex device structures, thick gate oxide and high voltage stress, high voltage CMOS devices exhibit usually high parasitics, high on-resistance of the channel and significant physical side effects such as HCI, junction leakage current, electromigration, self-heating effects etc. They are also more sensitive to PVT (Process, Voltage, Temperature) variations and have lower linearity and matching performance. The parameter Ltacc (Life time acceleration factor) is used to quantize the reduction of the life time of high voltage devices under different operating conditions. The layout size of high voltage devices is much larger, because guard rings are obliged to be included to avoid latch up effects and to ensure sufficient isolation between high voltage and low voltage circuit




a) Isolated low voltage MOSFETs b) High voltage sandwich capacitor

**Figure 2.9.:** Simplified cross sections of isolated low voltage NMOS and PMOS transistors and high voltage sandwich capacitor.

blocks on the same chip. The Source and Bulk terminals of high voltage transistors are tied together by default to reduce the body effect and latch up effect.

Integrated high voltage sandwich capacitors occupy large layout areas because of their low capacitance density and high parasitic capacitance to the p-substrate. The commonly used capacitor types in integrated circuits are double polysilicon capacitors, MIM (Metal-Insulator-Metal) capacitors, sandwich capacitors etc. Double polysilicon capacitors show the highest capacitance density but lowest maximum operating voltage at approximately 5 $V$, which are more suitable in low voltage and digital applications. MIM capacitors show the medium capacitance density with the medium breakdown voltage of about 20 $V$. Sandwich capacitors are currently the only available type of integrated capacitors providing maximum operating voltages of above 50 $V$ in high voltage CMOS technologies [Dat14c; Dat14g; Dat14d] .

Isolated low voltage transistors are able to provide the same good electrical performance (low threshold voltage, low on-resistance of the channel, small layout size etc.) like those in standard CMOS processes and work safely under high voltage operating conditions, as long as the voltage difference between each terminal is lower than their maximum allowed operating voltages, typically 5.5 $V$.

## 2.3 Level of Integration

Circuit analysis shows usually the feasibility to realize certain functionalities by means of different circuit architectures. Using discrete components, theoretical analysis can easily lead to a satisfying design. With optimized circuit architectures, the number of ICs and discrete components such as diodes and resistors can be reduced in order to achieve smaller PCB area and lower production costs. However, significant reduction of the overall size of the circuit can never be reached without considering the integration level of adopted ICs. Production costs including hardware costs, assembling costs etc. are dependent mainly on the number of ICs and discrete components. Higher level of integration requries a lower number of ICs and discrete components. Eventually, monolithically integrated circuits, for example, SoCs, can be designed to replace huge and costly PCB circuits. Therefore, the level of integration is a very important criterion during the selection of circuit architectures in analog IC design.

When designing integrated DC-DC converters for the high voltage generation, it is also more reasonable to choose a circuit architecture with higher level of integration. Considering production

costs, circuit performance and complexity play a secondary role compared with the integration level of the circuit.

### 2.3.1 Integrated Boost Converter

The basic circuit of boost converter has been already displayed in Figure 2.1. With its simple architecture, the integration level of boost converter can be investigated by analyzing each component.

- **Inductor:** Inductor-based DC-DC converters such as boost converter require high quality inductors to increase the power efficiency and voltage conversion ratio. The demanded inductors should provide high inductance and low ESR at their operating frequencies. A boost converter generating voltages beyond $100\,V$ from the $3.7\,V$ input voltage needs theoretically an inductor of at least several hundred microhenry with clock frequencies below $100\,MHz$. Discrete inductors such as SMD (Surface Mounted Device) inductors for high voltage applications occupy commonly footprints of above $10\,mm^2$ and they are especially bulky. The height of such components can be a couple of millimeter, which is not suitable for compact packaging of the whole circuit. Due to the technological limitation in current CMOS technologies, on-chip spiral inductors with only a few nanohenry for operating frequencies above $1\,GHz$ are able to be fabricated, although the necessary chip area is already unacceptably large [HG10]. With the help of additional magnetic cores, the inductance of these spiral inductors can be increased to several hundred nanohenry. However, the required chip areas remain very large and their fabrication in CMOS technologies is very complicated and expensive, which is usually not compatible with standard CMOS processes [DM09; KK13; MO09]. Another option is to use the inductance of bondwires as the replacement for integrated spiral inductors of low quality [WS07]. However, such methods belong no longer to the on-chip integration and it is difficult to implement inductors with high precision and stability by bondwires.

- **Diode:** The available diodes in current CMOS technologies are mostly parasitic diodes (parasitic pn-junctions) which require large chip area but show less performance such as low saturation current, low reverse breakdown voltage etc. They are not supposed to be used as standard devices and also not exactly modeled in the design kits provided by foundries. Designers must take their own risk, when adopting such parasitic diodes. If boost converter is designed to generate voltages above $100\,V$, the employed diode shown in Figure 2.1 should also be able to exhibit at least $100\,V$ reverse breakdown voltage. However, parasitic diodes with high breakdown voltages in current CMOS technologies show even worse performance than those low voltage ones [Dat14c; Dat14b; Dat14g; Dat14d]. The maximum allowed currents through those high voltage parasitic diodes are rather low. To provide sufficient high output currents, several high voltage parasitic diodes should be connected in parallel. This results however in unacceptable chip sizes. Diode-connected transistors with shorted Gate and Drain terminals can be only applied, where the maximum voltage difference between Gate and Source terminals are kept below the breakdown voltage between Gate and Source terminals, for example, maximum $20\,V$ for transistors with thick gate oxides in current CMOS technologies [Dat14c; Dat14b; Dat14g; Dat14c]. The most reasonable choice is to use discrete high voltage diodes in boost converter.

- **Switch:** Due to the simple circuit architecture of boost converter, only one high voltage switch is necessary. In current high voltage CMOS technologies, such high voltage transistors are well implemented in the form of LDMOS transistors with maximum breakdown voltages of up to $120\,V$ [Dat14c]. Even if the layout area of high voltage transistors is due to their complex structures and huge guard rings much larger than those of low voltage transistors, the required chip area for a single high voltage transistor can be still accepted. Such high voltage transistors

can handle maximum switching frequencies of several hundred megaherz and also exhibit saturation currents of several hundred milliampere.

- **Capacitor:** Capacitors are not necessary parts of boost converter, when the load is already capacitive. The purpose of the load capacitor $C_L$ in boost converter shown in Figure 2.1 is to maintain the output voltage $V_{out}$ and to reduce the output voltage ripple $\Delta V_{out}$, when boost converter is disconnected with the load during each clock period. If the load does not exhibit sufficiently high capacitance, a load capacitor of high capacitance value must be added to the output of boost converter. High voltage capacitors in current CMOS technologies have very low capacitance density but significant parasitic capacitors and resistors. For example, to build a high voltage capacitor of $1\,nF$ for operating voltages above $100\,V$, a layout area of about $8\,mm^2$ is needed in the high voltage CMOS technology H35 [Dat14c]. Due to the high ESR of these integrated high voltage capacitors, the output voltage ripple $\Delta V_{out}$ can only be limitedly reduced.

The difficulties to achieve the full integration of boost converter are dependent on the required inductor, diode and capacitor. In order to optimize voltage performance, most commercial ICs of boost converter in the market include merely high voltage switches and other basic analog blocks such as amplifiers, comparators etc. These ICs operate together with external discrete inductors, diodes and capacitors to realize the function of boost converter. This leads inevitably to high production costs and large footprints on PCBs. Fully integrated boost converters can be only found in applications with low voltage conversion ratios, where inductors of nanohenry as well as low voltage capacitors and diodes are adopted [HN13].

### 2.3.2 Integrated Charge Pumps

The most parts of charge pump circuits are capacitors and switches. It indicates that theoretically all kinds of charge pumps can be fully integrated. However, due to the unequal complexity and performance of circuit architectures, different chip sizes will be required to achieve similar results. To avoid unnecessarily large chip sizes, a reasonable circuit architecture is very critical.

- **Diode:** Diodes are mostly not essential components in charge pumps. Even in Dickson charge pump shown in Figure 2.5, the diodes can be replaced by diode-connected MOS transistors, which provide better electrical performance. Low voltage diodes are sufficient to withstand the most voltage stresses in Dickson charge pump, when the stage voltage gain, namely the voltage difference between each neighboring stage remains low voltage, typically below $5.5\,V$. Some research work on the implementation of Dickson charge pump by using pn-junction diodes or polysilicon diodes in CMOS technologies were reported [KT02; BS09; KC07]. The drawbacks of such methods are that the fabricated diodes can still allow only very low saturation current and the voltage drop over each diode is still significant, usually about $0.7\,V$. In order to increase the voltage gain, diodes or diode-connected transistors should be avoided. This can be achieved by the introduction of advanced charge pump architectures such as Pelliconi charge pump shown in Figure 2.6.

- **Switch:** The number of switches in charge pump circuits are usually very high. Especially in applications for the high voltage generation from low voltage power supplies, the number of switches increases with the stage number. Different charge pump architectures require different types of transistors as switches. If the voltage difference between each terminal of transistors can always be maintained below high voltage levels, standard low voltage transistors or isolated low voltage transistors can be applied. Otherwise, only high voltage transistors can ensure a robust and reliable design. Considering the large layout areas of high voltage transistors, the number of such transistors should be minimized. Modification of existing charge

pump circuit architectures or even a completely new circuit architecture could be necessary to achieve the desired high output voltage.

- **Capacitor:** High voltage capacitors are basic components for high voltage charge pumps. The number of these high voltage capacitors also increase with the stage number, so that the main layout area can be used only for the implementation of these capacitors. The best way for a compact layout design is to choose suitable capacitor types according to operating conditions. For multistage charge pumps with different node voltages, reasonable capacitor types should be applied for optimized layout sizes and voltage performance.

Fully integrated charge pumps are already realized in low voltage domains, since there are no significant technical obstacles to implement charge pump architectures. The overall chip size is usually small, when low voltage components are applied and the number of such components is also very limited [CT12]. The challenges to achieve high voltage conversion ratios in high voltage domains using charge pumps are to control the required chip size under acceptable limits and to ensure a robust and reliable circuit against high voltage stresses. Suitable circuit architectures and correct components should be chosen. Some attempts were successfully proven by silicon measurements [LS12; Zl07]. However, they are commonly based on Dickson charge pump, whose voltage gain is significantly reduced by voltage drops of the adopted diodes or diode-connected MOS transistors. As a result, the output voltages of those charge pumps are limited to much lower than 100 $V$ in current CMOS technologies.

### 2.3.3 Comparison

The discussion between integrated boost converter and charge pumps shows that charge pump circuits are the most promising choice to achieve the monolithic integration of the high voltage generation. Although boost converter needs only a few components and is easy to be designed, its basic components such as high voltage diodes and high value inductors are difficult to be integrated on-chip using current CMOS technologies. Applications of boost converter are mostly still realized by partially integrated circuits with external inductors. Charge pumps have usually complex circuit architectures and a high number of components. However, all those necessary components can be monolithically integrated. Possible feedback regulation circuits in both circuit architectures are low voltage circuit blocks which can also be fully integrated.

The optimization regarding the layout size of charge pumps is a very important issue. The critical factor here is the necessary stage number to generate the required high output voltage. The stage voltage gain of charge pumps will normally not exceed available power supply voltages due to their architectures. Hence, high stage number must be used for high voltage conversion ratios. This results in more complex interconnections with additional layout areas. Different from boost converter with simple circuit structures, where input currents are directly provided by DC power supplies, charge pumps require usually sufficiently large clock buffers. The charge is mainly transferred from the clock drivers to the circuit, although such clock drivers are eventually supplied by applied DC power supplies. To reduce the voltage loss induced by these clock drivers, transistors with very high channel width are mandatory to be employed in the clock drivers, which leads to a further increased layout size of charge pumps. Once the fabrication costs of such fully integrated charge pumps with large chip sizes are no longer competent against those of discrete ones, an overall consideration regarding the circuit performance and production costs should be taken into account.

Due to the low value capacitors available in CMOS technologies, charge pumps can only provide relatively low output currents, normally maximum a couple of hundred milliampere in low voltage domains. In high voltage domains, the possible maximum output currents of charge pumps decrease even below 1 $mA$. This suggests that they are merely suitable for low power applications, where no

high load currents are demanded. In high power applications, partially integrated boost converter with external components still dominates.

## 2.4 Summary

This chapter presents an extensive study on the level of integration of different DC-DC converters for the high voltage generation. Basic circuit architectures such as boost converter, Dickson charge pump and Pelliconi charge pump are introduced and discussed. Based on the knowledge of these circuit architectures, each essential component of the circuits are analyzed regarding their integration levels. A detailed comparison between charge pumps and boost converter is given. As a result, charge pumps are considered to be the most promising solution for the on-chip high voltage generation in current CMOS technologies.

# 3 Design Methodology for On-chip High Voltage Generation

As high voltage CMOS technologies are gaining more and more importance due to their integration of low and high voltage circuit blocks, new requirements are necessary in the high voltage circuit design. Potential shortcomings of traditional low voltage analog design methodologies should be overcome, and new enhancements should be added in order to develop a more effective analog design methodology for high voltage applications [Hof+13]. Such design methodology is based on accurate device models provided by high voltage CMOS PDKs (Process Design Kit), which are able to describe the special behavior of high voltage devices.

## 3.1 Design Kits for High Voltage CMOS Technologies

Foundries provide usually accurate PDKs including specific data and script files for EDA (Electronic Design Automation) tools, which help circuit designers finishing their tasks more efficiently. Important components of PDKs are device models, standard cell libraries, technology files, PCells (Parameterized Cell), design rule files etc. PDKs support a full custom design flow from schematic entry to final layout verification. In PDKs for high voltage CMOS technologies, more features and complexity are required to enable a fast and robust design, especially with respect to parasitics and reliability. Detailed information about these PDKs can be found in design documents regarding process parameters, design rules, parasitics, element layouts etc.

### 3.1.1 Device Models

Since more complicated device structures are employed in high voltage CMOS technologies, conventional SPICE (Simulation Program with Integrated Circuit Emphasis) models for low voltage analog devices are no longer sufficient to describe high voltage device characteristics. High voltage asymmetrical LDMOSs introduced in Figure 2.8 from Section 2.2 or general symmetrical high voltage MOSFETs with additional drift region between Gate and Source terminals show different behaviors compared to low voltage transistors. Accurate models of high voltage devices in CMOS technologies should include all parasitics in the lateral and vertical directions, particularly the more significant parasitic currents into the p-substrate due to the lack of buried layers used in BCD technologies. Aging modeling to describe failure mechanisms such as HCI, TDDB, NBTI etc. in high voltage devices is also a necessary part of high voltage device models beside the common noise, matching and statistical modeling [See11].

Such degradation or reliability performance can be further supervised during circuit simulations using SOAC (Safe Operating Area Check) tools provided by most design kits for high voltage CMOS technologies [Doc14d]. These SOAs (Safe Operating Area) are mainly determined by terminal voltages of devices. The operation within SOAs can avoid an immediate destruction of devices. Nevertheless, the degradation of devices or large shifts in their electrical parameters can still occur within SOAs, which eventually reduces the life times of devices. The life times at different SOAs can be calculated according to LTacc, which is a function of the operating conditions. Normally, at operating conditions with an LTacc of 1 or at turn-off conditions, devices have a life time of at least 10 years during continuous operations (approximately 87600 hours) [See10]. Higher LTacc means reduced

life times. For instance, an LTacc of 100 corresponds to a life time of merely 876 hours. (100 times shorter in hours). An example of the LTacc is shown in Figure 3.1. It can be seen, that the related high voltage transistor has a normal life time of about 10 years, when it operates continuously at Area a, while its life time will be 2000 times shorter at the continuous operation in Area d. It implies that the operating areas of $V_{GS}$ and $V_{DS}$ with both higher positive voltage levels result in higher LTacc. The cause for reduced life times of high voltage devices lies mainly in physical effects such as HCI, self-heatings etc. However, the overall life time of devices experiencing various operating conditions during the switched-mode operation is difficult to be summarized. Designers have to estimate the overall life time by approximation. Any operating condition of devices outside given safe operating areas is strictly forbidden and will lead to a complete damage of devices because of permanent oxide breakdown[1]. Moreover, life times are only specified for devices with minimum channel length in design documents. Devices with higher channel length are expected to have longer life times due to the reduced electrical stresses, which can be estimated according to the given process documents [Dat14c; Dat14b; Dat14g; Dat14d; Dat14f]. In addition, the forward operation of parasitic diodes will be warned during SOAC. Circuit designers must determine by themselves whether these warnings can be ignored [Doc14a]. Hence, SOAC is strongly suggested during circuit simulations of high voltage ASICs by foundries to ensure a robust and reliable design. Nevertheless, the simulation time with enabled SOAC tools will be considerably extended.

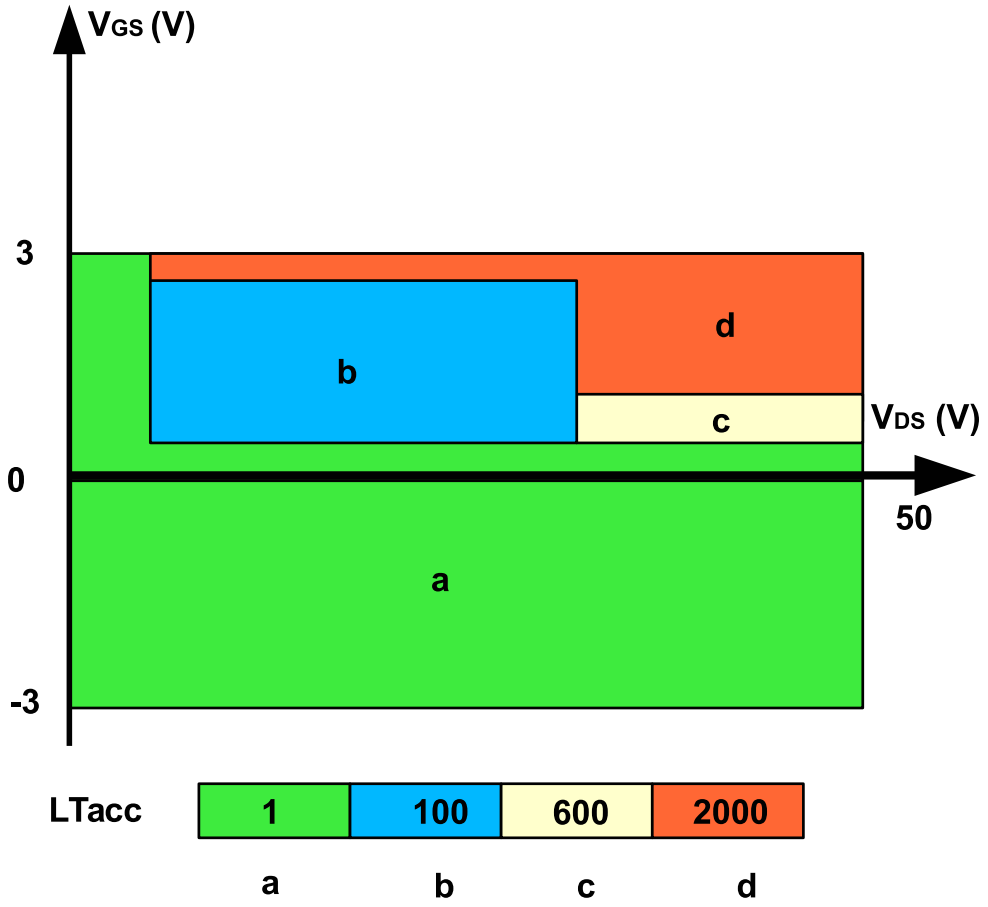



**Figure 3.1.:** Simplified SOA (Safe Operating Area) of a high voltage transistor [See10].

[1] Oxide breakdown is the most destructive for CMOS devices, while avalanche effects in pn-junctions and punch-through usually do not cause permanent damage of devices.

To achieve highly accurate models of high voltage devices with sophisticated structures, advanced SPICE models such as HiSIM-HV (extension of HiSIM, Hiroshima-university STARC IGFET Model) and MM20 (MOS Model 20) HVMOS (High Voltage MOS) model etc. were developed [GG10], in which high voltage features of devices are included. With the introduction of subcircuits to model high voltage phenomena, traditional SPICE models such BSIM (Berkeley Short-channel IGFET Model) are also able to characterize high voltage devices with acceptable precision [See11].

The mostly applied high voltage device models are:

- **BSIM-based model:** It is the extension of standard BSIM models for low voltage devices. Subcircuits are added to describe special characteristics of high voltage devices. For example, additional JFETs are used to represent the parasitic bipolar transistor in the p-substrate, which is responsible for the current injection into the p-substrate. Additional resistors are intended to specify the resistance of the drift region in LDMOSs. With this approach, special physical effects of high voltage devices can be included into the model. The drawbacks of BSIM-based models are that complex subcircuits are usually necessary for high voltage devices with complicated structures. Besides, the accuracy improvement by auxiliary subcircuits has a limitation, which is insufficient for highly demanding applications [See11].

- **HiSIM-HV model:** The HiSIM-HV model is selected as the industry-standard model for high voltage devices, because it is able to describe high voltage MOSFET behaviors accurately with a single global parameter set and without any aid of extra subcircuits. It includes all effects observed in state-of-art symmetrical and asymmetrical high voltage MOSFETs [GG10].

Experimental results in [Min11; Sch+08; Doc14d; See11; See10] have proven that HiSIM-HV models show better accuracy and speed than those BSIM-based models.

### 3.1.2 Figures of Merit

Some important figures of merit in high voltage CMOS technologies were concluded in [Min11]. They can be explained in a more detailed manner:

The choice of CMOS technologies for high voltage applications is mainly based on these figures of merit. Design kits of the chosen high voltage CMOS technologies should represent device characteristics precisely, particularly high voltage devices such as LDMOSs.

- **Maximum operating voltage:** It describes the maximum allowed voltage stress between the Drain and Source terminal of available high voltage transistors. Other passive devices such as capacitors, resistors etc. should also fulfill this maximum allowed operating condition. Besides, the duration of the maximum operating conditions affects the life time of high voltage devices, which must be considered and checked by SOAC tools in design kits for the sake of the reliability of high voltage devices against all possible transient voltage overshoots.

- **On-resistance:** The most applications of high voltage CMOS technologies are in integrated power management systems, where high voltage transistors are used as switches. These transistors such as LDMOSs exhibit high on-resistance mainly due to their large-sized device structures with long channel. Therefore, the on-resistance should be minimized by means of increased drift region doping level, enlarged channel width etc. to increase power efficiency and to decrease voltage drops across switches. Low voltage devices are also included in high voltage CMOS processes, whose on-resistance are of similar low values compared to those in standard CMOS processes.

- **Process complexity:** On one hand, high voltage CMOS technologies should have high process complexity to offer a variety of standard low voltage devices and special high voltage devices.

The possibility to adopt existing IP blocks directly is further helpful. Designs of complicated SoCs need support from such technologies with high process complexity. On the other hand, more complex processes require also more masks, which will increase overall chip production costs. To choose the most suitable technologies for concrete design tasks, balance between available devices and process costs should always be considered.

- **Process flexibility and extensibility:** To use designed circuits in different operating areas, high voltage CMOS technologies should have a wide range of operating voltages. For example, designs using the $0.35\,\mu m$ technology H35 for $50\,V$ applications can be extended with small changes of the used devices to up to $120\,V$ operating conditions [Dat14c]. This helps circuit designers greatly to apply existing circuits with less additional work in more applications.

In order to choose the most suitable high voltage CMOS technology, these 4 figures of merit should be taken into account. Related technology information can be found in design documents provided by foundries and checked through design kits in EDA tools.

## 3.2 Design Flow for High Voltage CMOS ASICs

The development of high voltage CMOS ASICs is more sophisticated than that of standard (low voltage) analog ASICs because of the specific characteristics of high voltage devices. The design flow for standard analog ASICs focuses mainly on the realization of electrical performance by means of basic design steps such as electrical design, physical design, test design etc. However, such design flow is no longer adequate in high voltage CMOS ASIC design without consideration of the large layout sizes and high operating voltages of high voltage devices. High voltage devices occupy commonly the most chip area compared with digital and low voltage devices. The physical isolation between low voltage and high voltage parts is also very important to reduce undesired interaction and to avoid catastrophic destruction of devices.

In [Doc14d], a design flow was proposed for the high voltage ASIC design. However, this suggested design flow still follows standard analog design flows with a few additional SOAC steps. Besides, this design flow is presented in the form of design steps using EDA tools, which does not show any concrete design considerations regarding high voltage circuits. These drawbacks are overcome by the design flow proposed in this work for high voltage CMOS ASICs shown in Figure 3.2, which discusses important procedures during the high voltage CMOS ASIC design and gives a clear prediction with respect to the design specification, feasibility and reliability of high voltage CMOS ASICs [Hof+13].

### 3.2.1 Design Steps

The proposed design flow for high voltage CMOS ASICs with design considerations about high voltage devices can be explained by the following steps:

- **Circuit topology selection:** This is the first design step after functional specifications are determined. Different from low voltage analog ASICs, many classic circuit topologies are no longer applicable to realize required functional specifications in high voltage applications due to the extremely high voltage stresses. Maximum operating conditions of each device should be considered and assured by estimation during the entire operation. Modification of existing circuit topologies or even a complete new circuit topology may be necessary to fulfill the reliability requirement. Besides, based on the knowledge of the large layout sizes of high voltage devices (transistors, capacitors etc.), circuit topologies with a high number of high voltage devices could be impractical for the monolithic integration, which may lead to an unacceptably

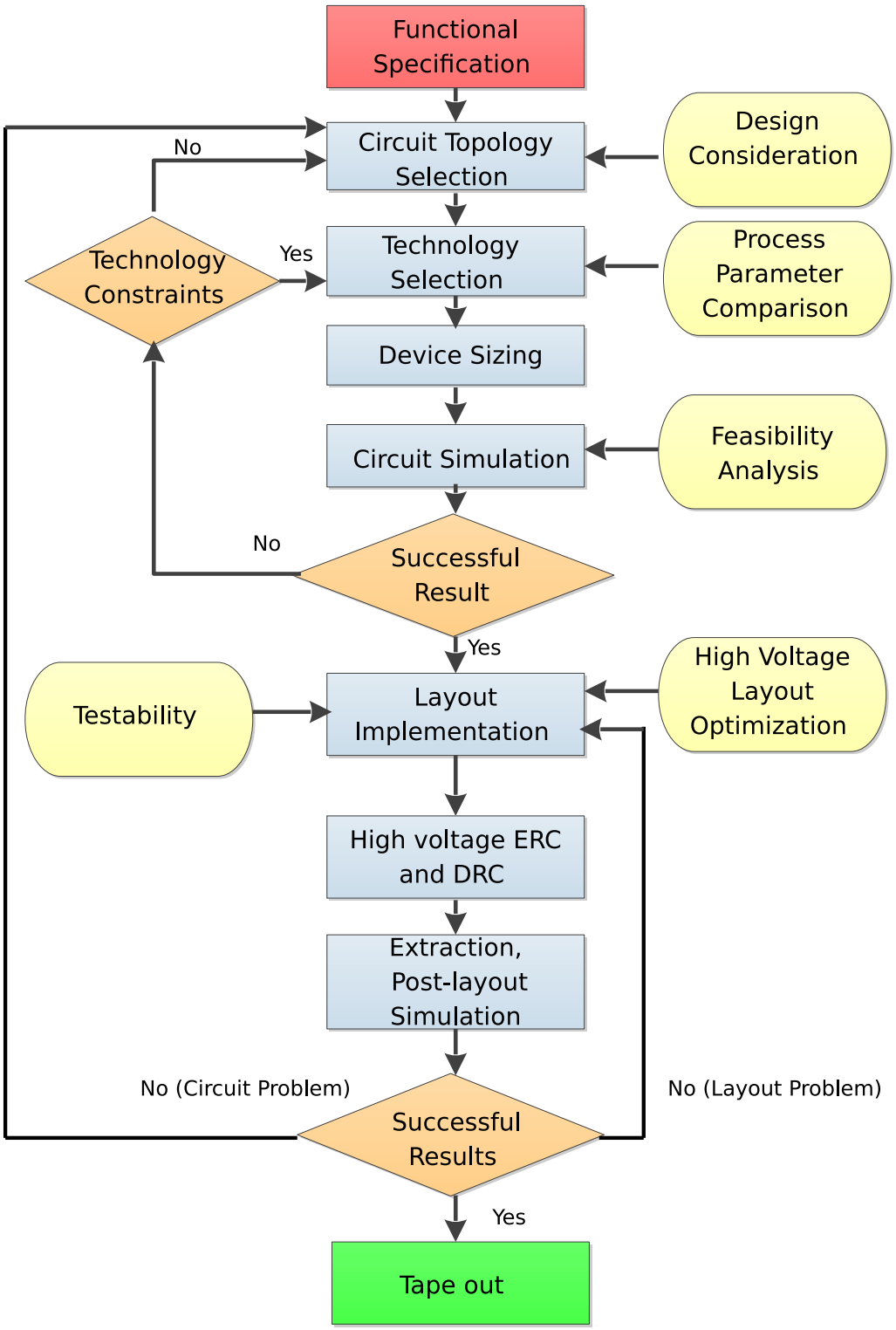



**Figure 3.2.:** Proposed design flow for high voltage CMOS ASICs.

large chip size. The feasibility of the integration of certain passive devices such as inductors, diodes etc. should also be taken into account. The decision between a fully integrated solution or a partially integrated solution with discrete components should be made in order to avoid unnecessary later redesigns. Advanced packaging, namely SiP (Sytem-in-Package) can be very useful to realize the decided circuit topology in a compact way. Especially, by using 3D (Three-Dimensional) integration, different parts of the circuit topology can be divided into several stacked chips, so that a small footprint of the entire package on PCBs can be achieved. However, not only the reliability and feasibility of circuit topologies regarding high voltage stresses and layout sizes but the production costs have also impact on the decision. The high cost of advanced packaging technologies is commonly an obstacle. Furthermore, another important aspect of the chosen circuit topology, namely the number of I/O pads should be considered dependent on whether the design is core limited or pad limited. In general, the reliability and feasibility of circuit topologies are more critical than the given functional specifications in the high voltage CMOS ASIC design. Hence, tradeoffs are usually unavoidable.

- **Technology selection:** Based on the determined circuit topology and given operating conditions, the most suitable high voltage CMOS technology should be chosen. The figures of merit discussed in Section 3.1.2 are used to compare different technologies. Firstly, a suitable high voltage CMOS technology should be able to provide reliable high voltage devices to support the chosen circuit topology under the required high voltage operating conditions. CMOS technologies with higher technology dimensions have usually higher maximum operating voltages. They need however also larger layout size to realize the chosen circuit topology. When providing sufficiently high operating voltages, technologies with smaller technology dimensions are preferred due to more compact layout sizes and lower production costs. The life times of high voltage devices under the required operating conditions should be considered. The estimation of the life time can be calculated in the form of LTacc provided by design documents. Reduced life times of devices imply also reduced life times of the whole circuit. Secondly, lowest possible on-resistance and parasitics of devices can significantly increase power efficiency and other electrical performance of the circuit. Thirdly, a wide choice of available low and high voltage devices can be further very beneficial to reach the given functional specifications. The possibility to use available standard analog cells and IP (Intellectual Property) blocks such as voltage references, comparators, amplifiers etc. will accelerate the entire design procedure. The extensibility of the technology can be additionally considered at last, if necessary.

- **Device sizing:** This step is very important, since the electrical performance and layout size of the circuit are determined by its applied devices and their sizes. From the available devices in the chosen technology, the suitable ones can be chosen according to the required operating conditions in the determined circuit topology. The sizes of the selected devices depend mainly on the hand calculation during the design. The device sizes can be optimized in the later circuit simulation step.

- **Circuit simulation:** After the decision on device sizes in the suitable circuit topology and high voltage CMOS technology, circuits with concrete devices offered by design kits of chosen technologies can be simulated in EDA tools in order to verify the correctness of the decision. Foundries are supposed to provide accurate device models. Self-developed devices are usually not supported. During the simulation, the dimension of devices should be determined by their maximum peak currents and voltages during the operation. However, electromigration of metal wires can not be simulated during schematic simulations, which should be handled during the layout design. If external discrete devices are included in the circuit, the precise modeling of such discrete devices is very important and sometimes needs to be modeled by circuit designers. Accurate models of load conditions are also necessary for a robust and reliable design, because in high voltage applications, small difference in load conditions may lead

to large difference in output currents and voltages. Margins of tolerance for load conditions should be simulated to ensure that the design is still robust and adequately accurate under unstable load conditions. High voltage circuits are usually simulated in DC or transient simulations, which implies that the required simulation time is rather long, especially when low voltage and high voltage circuit blocks are cosimulated. The reduction of the error tolerance in simulators of EDA tools can accelerate the simulations in certain degree, but the precision of the simulation results will be reduced. Such risks must be taken into account. Statistical simulations such as Monte Caro simulations, corner simulations, worst case simulations etc. are further necessary steps to verify the design under different PVT variations. The most important step at schematic simulation of high voltage circuits is to perform the SOAC, which is extremely time-consuming. At least one complete run of the SOAC for each possible operating condition must be conducted. Related warnings and errors shown by SOAC tools should be analyzed regarding the reliability of devices. If schematic simulation results with the SOAC do not meet given specifications, a modified or new circuit topology should be chosen. If failure or unreliability of the circuit occurs at the SOAC results, other devices or even another high voltage CMOS technology should be considered. After final schematic simulation with the SOAC, I/O cells with ESD (Electrostatic Discharge) protection circuits should be added, which should have nearly no influence on the circuit performance during normal operations.

- **Layout implementation:** It realizes the schematic circuit physically, which has been proven by the former steps to be feasible and reliable. Beside standard layout techniques for low voltage analog circuits regarding the improvement of matching and noise performance, the optimization of layout areas of high voltage devices is also very crucial. These high voltage devices occupy usually large layout areas, which may lead to an unacceptably large chip size. Guard rings are a necessary part of high voltage devices in order to avoid latchup and to provide sufficient isolation between circuit blocks with different operating voltages [Hol07; Doc14c]. After the optimization of each circuit block, reasonable placement of low and high voltage blocks will further simplify the wiring and reduce the overall chip size[2]. For all available devices and cells, Pcells included in design kits are supposed to be used to generate required layouts. Important parameters of device layouts such as width, length, substrate contacts can be adjusted in Pcells. The limitation of Pcells is that not all required devices are developed and provided in the form of Pcells. Pcells can be flattened and modified according to related design rules, which demands however a full understanding of high voltage CMOS technologies. Furthermore, any modification of given standard cells is not fully supported and guaranteed by foundries. Metal lines and interconnections should be designed carefully regarding their peak currents, since there is commonly no information about electromigration in design kits. In comparison to low voltage I/O cells, high voltage ones have large layout sizes, whose number should be minimized. In addition, it is strongly recommended to place probe pads at critical places inside chip layouts. This helps during later silicon measurements in the case of unexpected failures. Since the estimation of possible layout sizes was already performed during the circuit topology and technology selection, the final chip layout will usually not be quite different from the expected size.

- **High voltage ERC and DRC:** Tools and files for high voltage ERC (Electrical Rule Check) and DRC (Design Rule Check) are provided in all design kits. After the layout implementation of the circuit, a complete check by the ERC and DRC tools should be performed to make sure that the designed layout fulfills all the high voltage and low voltage design rules. Design rules for high voltage devices have normally higher requirements regarding the minimum width, separation and overlap of different layers. All design rule errors must be corrected by optimizing the layout. The listed notices and warnings should be analyzed by designers with respect to the

[2] Special aspects and techniques regarding the layout design of high voltage circuits are explained in Section 3.3.

potential unreliability of the design. Since the reliability is the most important specification in the high voltage circuit design, all the ERC and DRC errors must be solved. The responsible design support teams of foundries will be helpful to solve difficult problems related to ERC and DRC results. Before the parasitic extraction in the next step, a successful LVS (Layout versus Schematic) check is mandatory to ensure a correct translation of the schematic circuits into the physical layouts.

- **Extraction and post-layout simulation:** The parasitic extraction adds parasitic components such as resistors, capacitors etc. into the netlist file considering the parasitic effects between devices and layers in the layout. The parasitic extraction of high voltage circuits is similar to that of standard analog circuits. The post-layout simulation for high voltage circuits is however much more time-consuming than the schematic one. Especially for post-layout transient simulations, one simulation run may take a couple of weeks depending on the circuit size and computing powers of servers. Reduced parasitics during the parasitic extraction can be advantageous to accelerate the post-layout simulation with consideration about other sensitive circuit blocks such as oscillators, digital-analog-converters etc. Generally, a complete SOAC during the post-layout simulation is almost not possible due to limited time and server resources. As long as LVS check is successful, schematic simulation results with the SOAC are sufficient to guarantee the reliable operation of the circuit, since extracted parasitics in the post-layout simulation will mostly not affect the SOA of main devices. If the final post-layout simulation results fulfill all the requirements, database files such as GDSII (Graphical Design Station II) files can be generated and sent to the responsible foundry for the fabrication. However, if the final post-layout simulation results are inadequate, circuit designers must find out the causes. New layout implementations or even new circuit topology selections could be the solution.

### 3.2.2 Limitations

Again, this proposed design flow for high voltage CMOS ASICs focuses explicitly on the feasibility and reliability of the circuit, which are the most important design factors for high voltage fully or partially integrated circuits. Starting from the beginning of the design, possible chip size and reliability of devices are already taken into account. By concrete design considerations regarding high voltage constraints at each step, a robust and reliable ASIC with reasonable chip size can be achieved. Nevertheless, analog circuits can not be 100 % simulated by EDA tools in finite time, designers must determine an acceptable level of simulation results based on appropriate accuracy. Higher accuracy of simulation results requires longer simulation time. Hence, only the first test chip can prove the correctness of the design, where probe pads are supposed to help designers analyzing possible failures.

Considering current computing capability of computers, full chip simulation containing all low and high voltage circuit blocks is due to the long simulation time still difficult to perform. Each circuit block should be modeled accurately as equivalent interstage impedance or hardware description languages such as Verilog/Verilog-AMS models. Each circuit block can be simulated independently with reduced accuracy , but the required simulation time can be significantly minimized. Statistical simulations such as Monte Caro simulations regarding yield estimation are also impractical to be performed adequately because of their extremely long simulation time. Carefully selected but limited worst case simulations can be done to ensure that the designed circuits work still properly under the chosen worst operating conditions. For these reasons, further optimization can only be restrictedly continued. Due to the lack of modeling regarding effects of external magnetic fields in design kits, influences of operating environments are not considered in this design flow.

## 3.3 Layout Techniques for High Voltage CMOS ASICs

During the design of digital circuit layouts, two most important issues are the speed and area of devices, since digital applications are usually with high clock frequencies and a large number of devices. In the standard analog circuit design, the matching and noise of devices are however more important. With a small number of low voltage devices, the overall layout size of low voltage analog circuits will not be a great challenging in comparison with the accuracy of devices against mismatch and noise. Nevertheless, layout design techniques for high voltage analog circuits handle mainly the overall layout size and reliability of circuits against high voltage stresses. Although high voltage devices show worse matching and noise performance compared with low voltage ones, they can still meet the most design requirements because of their large layout size and consequently reduced device sensitivity.

### 3.3.1 Devices

High voltage devices are provided in the form of Pcells by design kits. By adjusting Pcells according to parameters such as channel width, channel length etc., required layouts will be automatically generated. It is strongly recommended to use the given Pcells, since foundries will mostly not support self-modified devices. Large high voltage transistors need to be splitted into multifinger transistors to achieve higher switching speed and more reasonable layout size. High voltage devices require large junction isolation, which results in large distance between devices. Guard rings to reduce substrate noises and latchup effects are mostly included in Pcells and can also be generated by available guard ring generators in design kits. Manuel drawing of guard rings requires a full understanding of high voltage CMOS design rules, which is normally not necessary. Devices with different operating voltages should be surrounded by guard rings of their voltage levels.

Head current problem in high voltage transistors should be considered, when the linearity becomes an important issue [Min11]. Head currents are defined as the currents which flow through the diffusion area from the Drain terminal to the Source terminal of high voltage transistors instead of through the channel, since in most high voltage transistors Drain terminals are implemented in the form of rings. Figure 3.3 shows the head currents inside high voltage transistors, where the total current is the sum of the current through the channel and the parasitic head currents through the diffusion area. Therefore, head currents influence the linearity of the device. Since head currents can not be completely eleminated due to the structure of high voltage transistors, they must be taken into account in applications requiring high linearity. Usually, wide high voltage transistors have relatively negligible head currents due to their significantly high channel currents. On the contrary, narrow high voltage transistors can be affected by those parasitic head currents, since their channel currents are relatively low [Min11].

Low voltage CMOS transistors in high voltage CMOS technologies occupy generally very small layout areas. There are two types of low voltage transistors available, namely non-isolated (bulk) transistors and isolated (floating) transistors. Classical non-isolated CMOS transistors are realized directly in the p-substrate, while isolated ones shown in Figure 2.9 from Section 2.2 are in the lightly doped deep NWELL. This deep NWELL must be biased by voltage levels higher than that of the p-substrate and provides high voltage offset. Non-isolated transistors can be only applied in low-side applications with considerable substrate leakage currents, while isolated ones can work in both high- and low-side applications with reduced substrate leakage currents due to the pn-isolation between the deep NWELL and p-substrate (see Figure 3.4). Therefore, it is usually preferred to use isolated transistors instead of non-isolated ones. Guard rings are normally demanded to be applied for the voltage isolation, especially when those low voltage devices are applied in high voltage applications.

Passive devices such as capacitors and resistors follow the standard layout design techniques for the matching and noise performance. In high voltage applications, guard rings are also required at

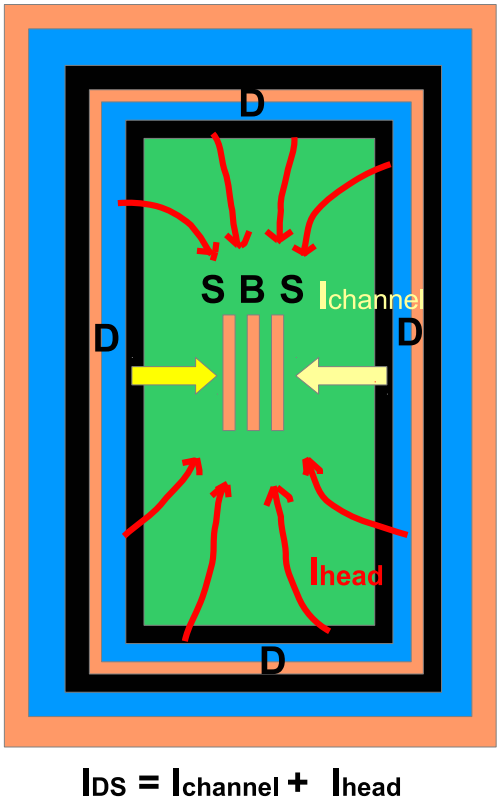
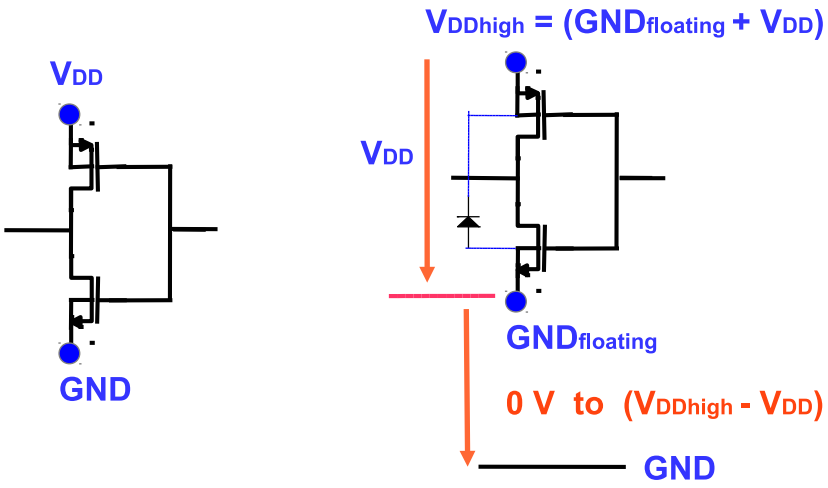



**Figure 3.3.:** Simplified head currents of a high voltage transistor [Min11].




a) Bulk CMOS transistors b) Isolated CMOS transistors

**Figure 3.4.:** Comparison between bulk CMOS transistors and isolated CMOS transistors.

these passive devices to reduce substrate noises and to provide sufficient isolation to low voltage circuit parts. Due to mechanical stresses, wide metal lines are not allowed in most technologies. As a result, high voltage capacitors of high capacitance values are implemented in the form of capacitor arrays composed of unit capacitors. Such passive devices can be placed over the deep NWELL to reduce substrate noises and to provide high offset voltages between each terminal and the p-substrate.

Multi-contacts are suggested to be adopted at any connection such as contacts at Gate terminals of transistors, contacts between different metal layers etc. in order to avoid fabrication defects and to reduce conduction resistance for the sake of the reliability.

It is evident that the chip size of most high voltage CMOS ASICs is determined by high voltage devices. It is not possible to achieve a compact chip layout by just putting devices together and routing them with metal lines. Both high and low voltage devices can be merged according to design rules for more compact layout size, which results in minimized parasitics as well [Has05]. Low voltage devices can be merged by standard methods such as sharing Drain or Source terminals of transistors, removing unnecessary contacts, minimizing distance between devices according to design rules etc., as long as devices operate still correctly and reliably against maximum peak currents and voltages. High voltage devices located in the same type of deep NWELLs/PWELLs under the same operating voltage can also be merged together with common voltage biasing [Doc14e]. Such voltage biasing in the (deep) NWELL is implemented by adequate contacts with metal layers, which have higher voltage levels than the p-substrate to maintain a reversed biased pn-junction. The deep NWELL is usually surrounded by a narrow p-type guard ring (deep PWELL) in the p-substrate to reduce sideways diffusion of the deep NWELL and to avoid over-doped regions in the p-substrate [Doc14e]. The deep NWELL has also different types according to their operating voltages depending on the doping concentration. The lightly doped deep NWELL is deeper than both the NWELL and the lightly doped deep PWELL in the p-substrate. The (deep) PWELL directly in the p-substrate should always have the same voltage level as that of the p-substrate, since no isolation junction in between exists. The (deep) PWELL placed inside the (deep) NWELL should be biased at lower voltage levels than those NWELLs to prevent the undesired conduction of the pn-junctions. Devices with huge (deep) NWELL or PWELL should be avoided, since high voltage drops will occur in consequence of the unequal voltage biasings. High voltage devices are usually large, therefore, empty areas of high voltage devices are strongly suggested to be filled with enough substrate contacts to reduce the substrate resistance [Doc14c]. Furthermore, guard rings with the same biasing voltage can also be merged, as long as enough contacts for the voltage biasing are maintained. In Figure 3.5, a simplified example of integration of high and low voltage devices is demonstrated, where distances between structures are approximately illustrated and necessary parts of devices such as guard rings, Drain and Source terminals etc. are omitted. Circuit blocks with different operating voltages such as $100\,V$, $20\,V$ and low voltage up to $5\,V$ are separated with each other by sufficient distance in the layout. Inside each circuit block, all the related devices can share the same deep NWELL, which leads to a more compact layout area. Nevertheless, the (deep) PWELL inside each deep NWELL should follow the design rules and keep enough distance with each other.

### 3.3.2 Layers

Since the vertical distance between different metal layers, namely the thickness of the dielectric in between is already determined by the chosen technologies, it is more important for designers to choose appropriate design techniques regarding the lateral distance between metal layers.

Polysilicon layers are not suitable for the signal routing due to their high resistance, which results in high latency and high power loss compared with metal layers [Doc14c]. At high voltage transistors, Gate terminals of polysilicon layers are preferred to be connected directly with metal layers by means of sufficient contacts in order to increase the speed of devices and to reduce dynamic power

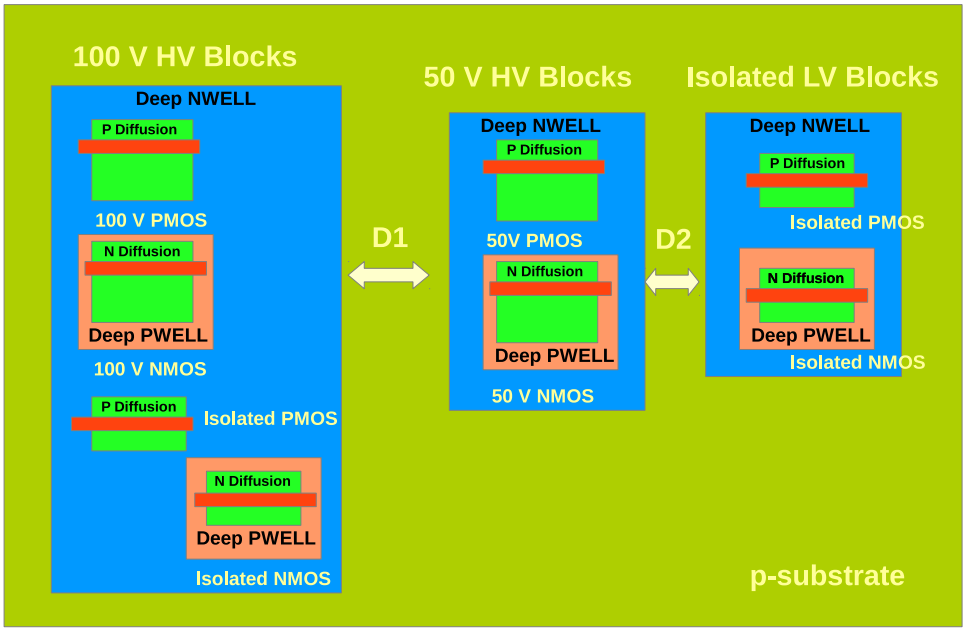



**Figure 3.5.:** Integration of different devices (HV: High Voltage, LV: Low Voltage).

loss. If thick metal layers are available, they are more suitable as power (high current) and ground lines due to their high saturation currents and low-ohmic resistance. Different thin metal layers can be connected together through adequate contacts to build conduction paths composed of multi-metal-layers with reduced resistance and increased saturation currents. For example, in the 0.35 $\mu m$ high voltage CMOS technology H35, Poly 1 and Poly 2 layers are not recommended for the signal routing. The Metal 1 layer is used for the routing inside each guard ring and between low voltage circuit parts. Thick Metal 4 layer is preferred for the routing of power supplies and high current paths. The rest Metal 2 and Metal 3 are used for the routing between circuit parts with different voltage levels [Doc14c].

Moreover, wide metal lines (e.g. wider than 35 $\mu m$) without any slots are generally due to thermal expansion and induced mechanical stresses not allowed [Dat14c; Dat14b; Dat14g; Dat14f] . Metal slots should be included in wide metal lines according to design rules. For each metal layer, certain minimum metal density (e.g. higher than 30 %) should be fulfilled, which is intended for the release of unnecessary mechanical stresses over the entire chip. Dummy metal lines could be useful to meet such requirements. The presence of wide metal lines with slots and minimum metal density will be checked by design kits during the DRC.

### 3.3.3 ESD Protection

ESD protection is always an important issue in integrated circuits. There are a variety of ESD structures to protect internal circuits from undesired ESD energy. In high voltage CMOS ASICs, circuits with multiple (low or high voltage) power supplies need multi-voltage ESD protection. I/O cells of different voltage levels require different ESD protection circuits. Power/ground cells require their suitable diode-based or MOSFET-based ESD clamp circuits. The highest voltage level inside the ASIC should always be kept through high voltage clamp circuits below the maximum operating voltage of chosen high voltage CMOS technologies. Isolated ESD protection circuits using isolated MOSFETs or triple-well diodes can significantly reduce the risk of latchup compared to non-isolated ones [Hol07].

I/O and power/ground cells belong to main external latchup sources, which may lead to minority carrier injection due to external charge, so that the parasitic BJT (Bipolar Junction Transistor) in the p-substrate will be turned on. Latchup risks in the internal circuitry are already reduced by the required guard rings and fulfilled design rules. ESD protection and clamp circuits for different voltage levels are mostly included in I/O and power/ground cells as standard cells in available design kits. Any modification of given ESD structures must follow the ESD design rules provided by foundries.

Figure 3.6 illustrates a possible ESD protection concept for high voltage CMOS ASICs with multiple power supplies [Doc14b]. Signals of different operating voltages have their own I/O pads, power/ground lines and ESD protection circuits according to their voltage levels. Diodes between different ground lines are so-called anti-parallel diodes, which are supposed to ensure a better common ground. In general, ESD protection circuits for higher operating voltages occupy larger layout sizes due to their larger ESD devices in comparison to lower voltage ESD protection circuits. For power and ground lines, thick metal layers are preferred to allow high peak currents. Additional capacitor arrays between power and ground lines will be helpful to stabilize the voltage levels of power supplies. Appropriate ESD clamp circuits regarding voltage levels of power lines are intended to avoid any voltage spike exceeding the maximum allowed operating voltages.

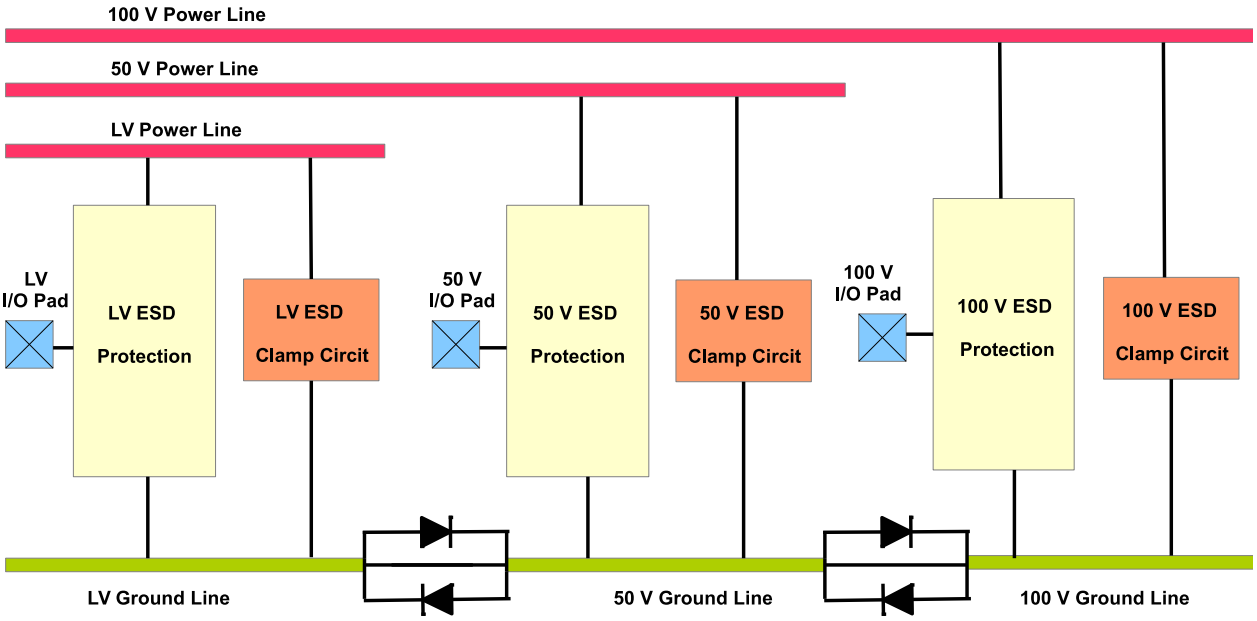



**Figure 3.6.:** ESD protection concept for multiple power supplies [Doc14b].

## 3.4 Monolithic Integration of CMOS High Voltage Generators

The design of step-up DC-DC converters in high voltage CMOS technologies follows the design flow proposed in Section 3.2. The layout techniques discussed in Section 3.3 are also applicable, since high voltage CMOS generators belong to high voltage CMOS ASICs. At the meantime, some special aspects of integrated high voltage CMOS generators should be taken into consideration, so that circuit optimization can be achieved based on the extensive understanding of the related design constraints.

### 3.4.1 System-on-Chip or System-in-Package

Before the decision is made between boost converters and charge pumps for the high voltage generation, technology constraints of high voltage CMOS processes need to be kept in mind. Passive components like capacitors and inductors can be only integrated with low quality and low values compared with those discrete ones. Moreover, these passive devices require considerable chip areas as well. Any modification of standard process steps for special devices such as MEMS, and any addition of specific materials such as magnetic materials for enhanced performance of devices like inductors are usually not possible or very expensive in CMOS technologies.

For boost converter, it is difficult in CMOS technologies to achieve on-chip high value inductors. Moreover, available low value inductors show significant power loss due to their high ESR and parasitic capacitance. High voltage diodes in CMOS technologies are mainly parasitic diodes, which are not able to meet current requirements in boost converter.

For charge pumps, it is not optimal to integrate large high voltage capacitors with low capacitance density, when the chip area is dominantly occupied by those high voltage capacitors. The overall production cost of fully integrated charge pumps should not exceed that of partially integrated solutions with discrete components. However, requirements for the monolithic integration of ICs in certain applications can play an important role despite high production costs.

The choice between SoC (System-on-Chip) and SiP (System-in-Package) needs to be considered with respect to tradeoffs among overall production costs (chip costs, packaging costs etc.), reliability, circuit performance and footprint on PCBs. Connections between different chips and discrete components in SiP regarding both 2D (Two-Dimensional) and 3D integration should be modeled and included during circuit simulations to obtain more precise simulation results.

### 3.4.2 Architecture Selection

Charge pumps have a variety of circuit topologies, while boost converter has only the simple one. The most important design factor of charge pumps for the high voltage generation is stage voltage gain. With higher stage voltage gain, the number of stages (capacitors, switches etc.) and the entire layout area will be reduced. Stage voltage gain can be improved by using advanced charge pump architectures. This improvement takes place by means of the reduction of the voltage drop across charge transfer switches and other voltage losses due to insufficient control of charge transfer switches.

For example, with Pelliconi charge pump architecture using MOS switches in Figure 2.6 from Section 2.1.2, the voltage drop across the charge transfer switches is significantly decreased compared with the diodes or diode-connected MOSFETs in Dickson charge pumps.

Furthermore, the reliability of circuit architectures in high voltage applications must be carefully taken into account, so that all the transistors, capacitors, inductors, diodes etc. always operate under their maximum allowed voltage and current limits.

### 3.4.3 Device Selection

Integrated planar inductors have only limited applications due to their low quality and low inductance. Inductors realized by bonding wires or discrete inductors are an alternative depending on design requirements. The choice of inductors determines considerably the overall power loss of boost converter. Inductors with high ESR are not desired, because they can lead to heating problems at high switching frequencies or high conduction currents.

Diodes can be implemented by diode-connected MOSFETs shown in Figure 2.4 from Section 2.1.2, whose reverse breakdown voltages between the equivalent cathode and anode equal breakdown

voltages between Gate and Source terminals of MOSFETs. This indicates that high voltage diodes above $20\,V$ can be hardly obtained by diode-connected MOSFETs in current CMOS technologies, since the breakdown voltages between Gate and Source terminals of MOSFETs with thick gate oxide are only maximum $20\,V$ according to [Dat14c; Dat14g; Dat14d]. Stacked diode-connected MOSFETs can be a solution to realize high voltage diodes for operations above $20\,V$, which require however larger chip area and result in higher voltage drops during their forward biased operation. Large-sized parasitic high voltage diodes provided in design kits usually operate under low conduction currents and are not suggested by foundries to be used as standard components.

Capacitors with lower maximum operating voltages exhibit mostly higher capacitance density and less parasitics. In multistage applications, it is beneficial to adopt capacitors with sufficient maximum operating voltages regarding voltage levels at the current stages. The avoidance of unnecessary high voltage capacitors can increase circuit performance and reduce chip area. In charge pump architectures, significant waste of charge takes place during the charging and discharging of the parasitic capacitors in pumping capacitors by clock drivers. Usually, parasitic capacitors at the terminal close to the p-substrate are much larger than those at the other terminal located at higher metal layers. Hence, different ways to connect high voltage capacitors regarding their terminals can influence the voltage gain and power efficiency of the circuit. Besides, oxide breakdown results in permanent damage for any device, which requires absolute safe operating conditions for high voltage capacitors. Due to the mechanical stress and thermal expansion of metal layers, the maximum allowed metal width is limited. High capacitor value is implemented by capacitor arrays with unit capacitors of a couple of hundred femtofarad, which is therefore discrete. The decision of capacitor values lies in tradeoffs between stage voltage gain, accuracy of capacitance and layout area.

In Section 2.2, low and high voltage devices in high voltage CMOS processes are already discussed. High voltage transistors with tied Source and Bulk terminals are not suitable for charge pump architectures, because the voltage levels at each side of MOS switches in charge pumps will be biased high and low alternatively, which leads to the conduction of parasitic body diodes of the MOS switches at each second half period. The large layout size of high voltage transistors also prevents their applications in charge pumps with high stage number. Isolated low voltage transistors with high voltage offset operate properly, when those transistors are always kept under their maximum allowed operating conditions both vertically (high voltage) and horizontally (low voltage). To use isolated low voltage transistors can diminish layout area and conduction loss. With serially connected isolated low voltage devices, the maximum breakdown voltage between Drain and Source terminals can be increased. However, the low breakdown voltage between Gate and Source terminals should always be taken into account. The channel width of switches is determined by the maximum current through the main current path. Switches for control signals need to be appropriately small, but switches for charge transfer or high conduction currents should be large enough.

### 3.4.4 Tradeoffs among Various Design Requirements

Design factors of charge pumps such as overall power efficiency, layout area, ramp-up time and recovery time of output voltage, output voltage ripple etc. are commonly considered after the optimization of stage voltage gain. To achieve the monolithic integration of high voltage charge pumps, to increase stage voltage gain is the most effective method to decrease the overall chip size. Besides, with optimized stage voltage gain, overall power efficiency and layout area can usually also be improved. To prioritize the optimization of power efficiency and layout area before stage voltage gain can result in lower stage voltage gain and higher stage number to reach the required output voltage, which will leads probably to a larger final chip size.

As for boost converter, although its architecture is very simple, some combination of boost converter and charge pumps can be considered to reduce the required inductor value and to decrease layout area. For instance, the input voltage of boost converter can be increased at first by a charge

pump, so that the required inductor value of boost converter will be lower (see Section 2.1.1). Such hybrid architectures composed of boost converter and charge pumps need however additional layout areas and consume extra power, which should be balanced carefully.

Similarly, additional circuits for charge pumps can also be added to enhance stage voltage gain or other design factors. The effects of those additional circuits on the overall performance such as layout area, power consumption etc. should be considered. For example, using increased clock voltage levels to reduce stage number and chip area seems helpful. However, another charge pump circuit as the high voltage level shifter with high switching frequencies and large pumping capacitors to ensure stable clock voltage levels must be integrated. The overall power efficiency and layout area will be probably affected.

During the design of high voltage generators, lots of tradeoffs should be made to meet the given specifications. Design requirements need to be listed and implemented according to their priorities.

### 3.4.5 Control Circuits

Control circuits of high voltage generators are necessary to decrease influences of unstable operating conditions such as load (output) and line (input) variations. They can not only ensure a stable output voltage but also protect high voltage devices from the reduction of their reliability. Generally, control circuits in integrated high voltage generators are supposed to be fast enough to react against changes of operating conditions. They should also be as low-power as possible. A simple architecture is preferred to reduce the required layout size. Typical control circuits are composed of resistive or capacitive voltage dividers, voltage references, error amplifiers etc.

The control methods for boost converter are mostly realized by PWM or PFM (Pulse Frequency Modulation), where the duty cycle or frequency of clock signals is controlled according to current output voltages [WS11].

Charge pumps can mainly be controlled by adjusting their clock frequencies to provide required stable output voltages. Nevertheless, it is also possible to regulate charge pumps by adjusting their conversion ratios and pumping capacitor values. Conversion ratios of charge pumps can be varied through switch-on and off of certain switches depending on circuit architectures. Pumping capacitor values can be modified dynamically by connecting or disconnecting certain unit capacitors inside each capacitor array, which implements the pumping capacitors at each stage.

Those control circuits contain mostly low voltage circuit blocks, which can be easily fully integrated with reasonably small chip sizes. Linear regulator is usually not suitable to stablize the output voltage in integrated high voltage generators due to its high static current consumption, low power efficiency etc. In spite of its simple architecture, it will significantly reduce the output voltage and overall power efficiency.

### 3.4.6 Clock Generation and Distribution

Precise on-chip multiphase clock generation is restricted by PVT variations. Some ring oscillator structures adopting differential delay cells show the possibility of stable clock generation [TT10]. The clock frequency is a function of the device size for delay generation and voltage amplitude of the oscillation. In most cases, off-chip clock sources provide more reliable performance.

The difficulty in clock distribution increases with the number of charge pump stages. Clock tree design for the exact implementation of each clock phase at each stage can be rather time and layout-area consuming. Compromises between clock precision and layout area are often necessary.

Noises in high voltage generators are due to the switching mechanism not avoidable. Guard rings are used to protect devices from noises, while noises around the clock signal path should be handled by dedicated layout techniques such as the use of shielding lines along with clock signals.

To achieve short rising/falling times of clock signals and to provide high currents from DC power supplies to pumping capacitors in charge pump circuits, on-chip tapered clock buffers are mostly indispensable. They are actually inverters of large sizes, whose power consumption is significant. Hence, the optimization of these inverters regarding static and dynamic power loss is very meaningful.

### 3.4.7 Challenges during Circuit Simulations

In the high voltage circuit design, the SOAC is essential to ensure that devices always work under their maximum allowed operating conditions. Any operating outside the SOA of devices leads to the damage of devices. High voltage generators contain usually switched capacitors or inductors, which require transient simulations up to a couple of hundred millisecond to reach stable states. The post-layout transient simulation of high voltage generators with the SOAC can take extremely long time by computers with limited processing power. As long as the LVS check is successful, schematic simulation results with the SOAC are sufficient to guarantee the reliable operation of devices, since extracted parasitics in post-layout simulation will mostly not affect the SOA of main devices. Reduced parasitics during parasitic extraction can be advantageous to accelerate the simulation. However, sensitive blocks such as oscillators, digital-analog-converters etc. will be affected during the simulation.

Even with reduced accuracy, the cosimulation of high and low voltage circuit blocks in the whole ASIC is still difficult to perform because of the long simulation time. Different corner simulations and Monte Caro simulations are supposed to be conducted to improve the robustness and reliability and to obtain yield prediction. But in reality, they have to be simplified due to limited simulation time. The changing of load conditions during the normal operating of the circuit is also not able to be sufficiently investigated, which has considerable influences on the reliability of the circuit but demands much simulation time. Moreover, the precision of device models is very critical for a successful design. It is still a great challenge to model high voltage devices of complicated structures and high parasitics precisely.

## 3.5 Summary

This chapter introduces design kits and device models provided by current high voltage CMOS technologies. The necessity of the SOAC to achieve a reliable and robust design is explained. A new design flow with focus on the feasibility and reliability of high voltage CMOS ASICs is proposed. Each design step in this proposed design flow is explained and analyzed in detail. Different useful layout techniques regarding devices, layers and ESD protection for high voltage applications are presented. At last, several design techniques for monolithic high voltage generators are given to discuss the important aspects such as architecture selection, device selection, challenges during the circuit simulation (mainly due to the extremely long simulation time) etc.

# 4 Design and Implementation of Fully Integrated High Voltage Charge Pumps

As already discussed in Chapter 2, charge pump architectures can be monolithically integrated in CMOS technologies and are capable of creating high voltages from low voltage power supplies. Therefore, instead of boost converter with bulky inductors, it is more convenient to integrate charge pumps monolithically or as parts of SoCs in high voltage applications. The two high voltage ASICs presented in this chapter are based on the design methodology and layout techniques discussed in Chapter 3.

## 4.1 Fully Integratable 4-phase Charge Pump Architectures for High Voltage Applications

The monolithic integration capability of charge pumps has drawn the attention of many researchers. This increased attention has resulted in a variety of circuit architectures to improve power efficiency, chip size, stage voltage gain etc. However, the most studies focused mainly on low voltage domains and were limited by the available CMOS technologies in the past. Some newly developed $0.35\,\mu m$ [Dat14c; Dat14g] and $0.18\,\mu m$ [Dat14b; Dat14f; MK10] technologies are competitive with the BCD and SOI technologies with respect to the fabrication cost and the process performance [PS11; Sch+08]. This development has also gained wide attention of researchers. In the current scenario, the reliability of high voltage generators while generating high voltage stresses has to be analyzed.

### 4.1.1 Drawbacks of Dickson Charge Pump

Dickson charge pump is considered as the most commonly used charge pump architecture in integrated DC-DC converters [Dic76; PP10] (see Section 2.1.2). Dickson charge pump utilizes diodes as charge transfer switches. Unfortunately, integrated diodes such as MOSFET body diodes provided in most CMOS technologies are typically parasitic diodes, which occupy large chip area and exhibit low saturation current density. For this reason, diode-connected MOSFETs with connected Drain and Gate terminals are used as the replacement of diodes in integrated Dickson charge pump circuits. Diode-connected MOSFETs will not conduct, unless the voltage difference between Drain (Gate) and Source terminals is higher than their threshold voltages, which is similar to the electrical behavior of diodes.

Considering the parasitic capacitor $C_s$ of the integrated pumping capacitor $C$, the output voltage $V_{out}$ of an $n$-stage Dickson charge pump shown in Figure 2.5 can be calculated according to Equation 4.1. The stage voltage gain $\Delta V$ and the output voltage ripple $V_{ripple}$ at the output capacitor $C_L$ can be calculated by using Equation 4.2 and 4.3, respectively [Dic76; PS06][1].

$$V_{out} = V_{dd} + nV_{clk}\frac{C}{(C+C_s)} - n\frac{I_L T}{(C+C_s)} - (n+1)V_{th}, \text{ where } V_{clk} = V_{dd} \tag{4.1}$$

$$\Delta V = V_{clk}\frac{C}{(C+C_s)} - \frac{I_L T}{(C+C_s)} - V_{th}, \text{ where } V_{clk} = V_{dd} \tag{4.2}$$

[1] $V_{dd}$ is the DC power supply. $V_{clk}$ is the voltage amplitude of clock signals. $I_L$ is the load current. $T$ is the clock period. $V_{th}$ is the threshold voltage of transistors.

$$V_{ripple} = \frac{I_L T}{C_L} \tag{4.3}$$

Equation 4.2 shows that the stage voltage gain $\Delta V$ is limited by the threshold voltage $V_{th}$. It is the voltage drop across the diode-connected MOSFETs during the forward conduction and its value is about $0.7\,V$. Therefore, Dickson charge pump requires a high stage number for high output voltages. With the increasing voltage difference $V_{sb}$ between Source and Bulk terminals of MOS transistors, the threshold voltage $V_{th}$ increases due to the body effect [PS06]. If the Bulk terminal is connected to the Source terminal to maintain $V_{sb} = 0\,V$ and to overcome the body effect, the parasitic body diodes of MOS transistors will conduct during the charge pump operation. This will reduce the reliability of devices. Hence, Bulk terminals of MOS transistors are usually connected to certain constant voltage levels to avoid the conduction of those parasitic body diodes. Especially at higher stages, the threshold voltage $V_{th}$ of MOS transistors will be very high. This leads to significantly reduced stage voltage gain $\Delta V$, and the whole circuit saturates at certain output voltage levels. Equation 4.3 shows the factors related to the output voltage ripple $V_{ripple}$. To minimize the output voltage ripple $V_{ripple}$, the output capacitor $C_L$ should be increased, whereas the values of the load current $I_L$ and the clock period $T$ should be reduced.

### 4.1.2 Drawbacks of Pelliconi Charge Pump

To overcome large voltage drops across diodes or diode-connected MOSFETs in Dickson charge pump, Pelliconi charge pump shown in Figure 2.6 from Section 2.1.2 was proposed. It employs control signals to actively operate the MOS switches in the circuit, while the diode-connected MOSFETs in the Dickson charge pump circuits are passively turned on and off by the voltage difference between Drain and Source terminals [PR03]. Since the voltage drop across each switch at Pelliconi charge pump is not the threshold voltage $V_{th}$ of MOS switches, compared to the Dickson charge pump circuits, but the normally very low conduction voltage drop of MOS switches, the stage voltage gain is considerably improved. Nevertheless, the requirements for the accuracy of control signals at each switch in Pelliconi charge pump are very high.

$$V_{out} = V_{dd} + n(V_{clk}\frac{C}{(C+C_s)} - \frac{I_L}{2f(C+C_s)}), \text{ where } V_{clk} = V_{dd} \tag{4.4}$$

$$\Delta V = (V_{clk}\frac{C}{(C+C_s)} - \frac{I_L}{2f(C+C_s)}), \text{ where } V_{clk} = V_{dd} \tag{4.5}$$

Figure 2.6 shows a single stage Pelliconi charge pump, in which the control signals at Node A and Node B switch on and off the NMOS (N-type Metal-Oxide-Semiconductor) and PMOS (P-type Metal-Oxide-Semiconductor) switches. In multistage Pelliconi charge pump, the voltage levels at Node A and B of each stage are charged up to certain voltage levels stage by stage through the two-phase non-overlapping clock signals $V_{clk}$ and $V_{clkB}$. Charge is transferred from the DC power supply $V_{dd}$ and clock buffers to the output of the circuit. Equation 4.4 and 4.5 indicate significantly higher stage voltage gain compared with Dickson charge pump circuits under the same operating conditions [PR03][2]. The body effect problem seems to be solved by connected Source and Bulk terminals of MOS switches. However, the parasitic body diodes of MOS switches will conduct during the charge transfer phase, which is usually not recommended and leads to the degraded robustness and reliability of devices. Moreover, the control signals at Node A and B need to be very precise

[2] $V_{dd}$ is the DC power supply. $V_{clk}$ is the voltage amplitude of clock signals. $I_L$ is the load current. $T$ is the clock period. $C_L$ is the load capacitor. $C_s$ is the parasitic capacitor of the integrated pumping capacitor $C$.

in terms of timing and voltage levels. In reality, the non-ideal control signals of the MOS switches result in large reverse currents through the both conducting NMOS and PMOS transistors from higher stages to lower stages at each clock switching time [WTK10]. Consequently, the stage voltage gain and power efficiency of the circuit are decreased.

### 4.1.3 Drawbacks of Heap Charge Pump

Heap charge pump, also called series-parallel charge pump, is another type of charge pumps, which can convert low input voltages to high output voltages [ABT05; TT11]. Figure 4.1 shows the basic concept of a 4-stage heap charge pump powered by an input voltage $V_{dd}$, which can ideally generate high output voltage by changing the circuit topology. Ideally, in the first half clock period, all the 4 capacitors will be charged up to $V_{dd}$. In the second half clock period, all the 4 capacitors will be stacked and the output voltage $V_{out}$ will be increased to $5V_{dd}$. Similarly, in ideal cases for an n-stage heap charge pump, $V_{out} = (n+1)V_{dd}$. The advantages of heap charge pump are that it requires no large clock buffers, since clock signals are used as control signals of the switches instead of sources of charge. Hence, the chip area can be saved and power efficiency will be increased. Theoretically, the output voltage $V_{out}$ can reach its maximum value $(n+1)V_{dd}$ after the first clock period, which is more rapid than other types of charge pumps. It can be seen that the output of heap charge pump should be disconnected by diodes or diode-connected MOSFETs with the load, when the capacitors are being charged by the DC power supply $V_{dd}$. Otherwise, the output voltage will have large voltage swings.

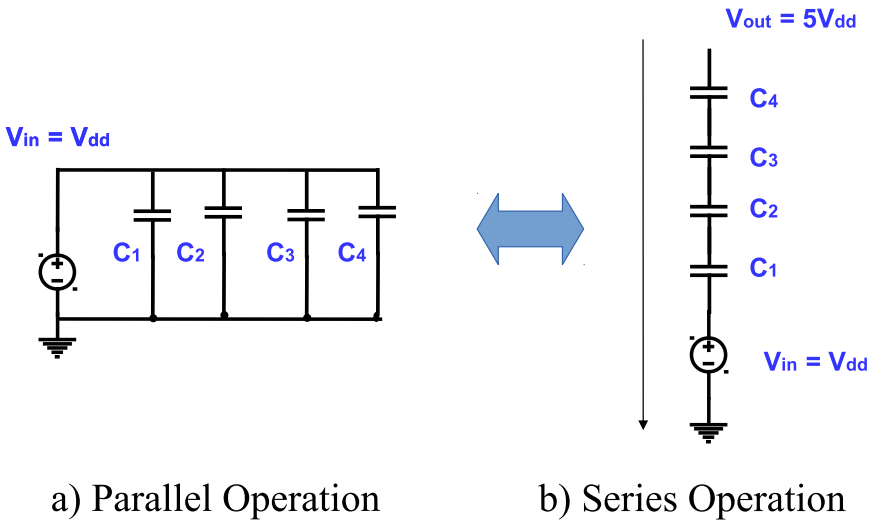



**Figure 4.1.:** Concept of a 4-stage heap charge pump [TT11].

In reality, the series and parallel connection of pumping capacitors are realized by switches, which introduces voltage drops and additional resistors. During the charging phase, each pumping capacitor can not be fully charged up to $V_{dd}$. And during the charge transfer phase, the output voltage $V_{out}$ is also reduced by the voltage drops across the switches in the charge transfer path. Due to the induced RC delays, the output voltage $V_{out}$ usually can not be increased to its maximum value during the first clock period. Considering the parasitic capacitors of pumping capacitors, especially the large bottom plate parasitic capacitors, charge at each pumping capacitor will be mostly wasted by these parasitic capacitors, which reduces the voltage gain significantly (see Figure 4.2).

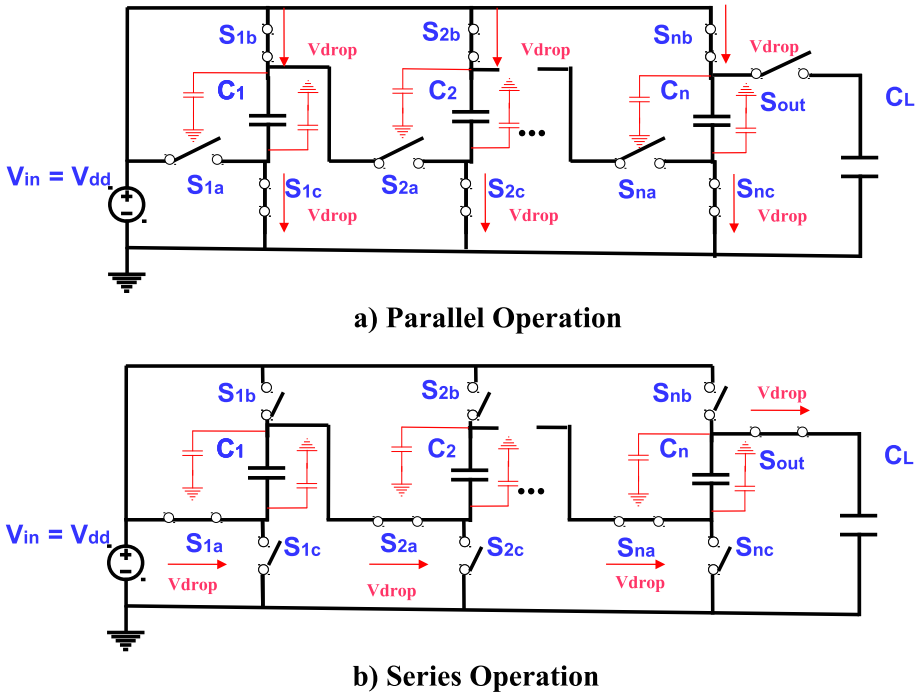



**Figure 4.2.:** Circuit diagram of an n-stage heap charge pump including parasitics [ABT05].

The difficulties to use heap charge pump for high voltage generation in CMOS technologies are not only the non-ideality of switches and pumping capacitors, which leads to reduced voltage gain, but also the required high voltage control signals for the switches at higher stages. The available low voltage clock signals are not sufficient to control the switches. Therefore, heap charge pump is usually used in low voltage applications (below $5\,V$), where clock signals are able to directly switch on and off each switch. It ensures that the voltage difference between Gate and Source terminals of each MOS switch is kept below their breakdown voltages [TT11].

In [Reu13], an innovative heap charge pump architecture driven by 2-phase non-overlapping clock signals $V_{clk}$ and $V_{clkB}$ was proposed (see Figure 4.3). The necessary control signals for switches at higher stages (PMOS switches in the charge transfer path) are realized by the switching voltage levels at the former stages. A single stage Dickson charge pump is adopted to generate the control signals for the NMOS switches above, while the NMOS switches below are directly controlled by clock signals. Using discrete components such as $1\,\mu F$ pumping capacitors, high voltage NMOS and PMOS switches, high voltage diodes etc., a 9-stage heap charge pump based on this proposed architecture can generate approximately $50\,V$ from $5\,V$ DC power supply without load resistors. However, for the realization of this architecture in CMOS technologies, many problems need to be solved. First of all, the high voltage diode $D_2$ shown in Figure 4.3 can hardly be integrated on-chip, since it requires very high reverse breakdown voltage and diode-connected MOSFETs in current CMOS technologies can withstand maximum $20\,V$ reverse breakdown voltage [Dat14c; Dat14b; Dat14g; Dat14f]. Diode-connected MOSFETs have connected Gate and Drain terminals, which indicates that the reverse breakdown voltage of the equivalent diodes equals the breakdown voltage between Gate and Source terminals. In current CMOS technologies, MOSFETs with thick gate oxide have a breakdown voltage between Gate and Source terminals lower than $20\,V$. Parasitic high voltage diodes in CMOS technologies are not suggested to be used as standard components for the sake of reliability. Secondly, when the values of pumping capacitors are reduced to several picofarad, the influences of

the parasitic capacitors of those pumping capacitors will be significant, so that the output voltage remains at a very low voltage level. This is also the case, when load resistors are applied, because series pumping capacitors of several picofarad are too small to provide sufficient load currents. Furthermore, in this architecture, almost all the transistors are high voltage transistors to withstand high voltage stresses. The layout area for a high number of stages will be unacceptably large, so that the integration of this architecture in CMOS technologies becomes no longer meaningful.

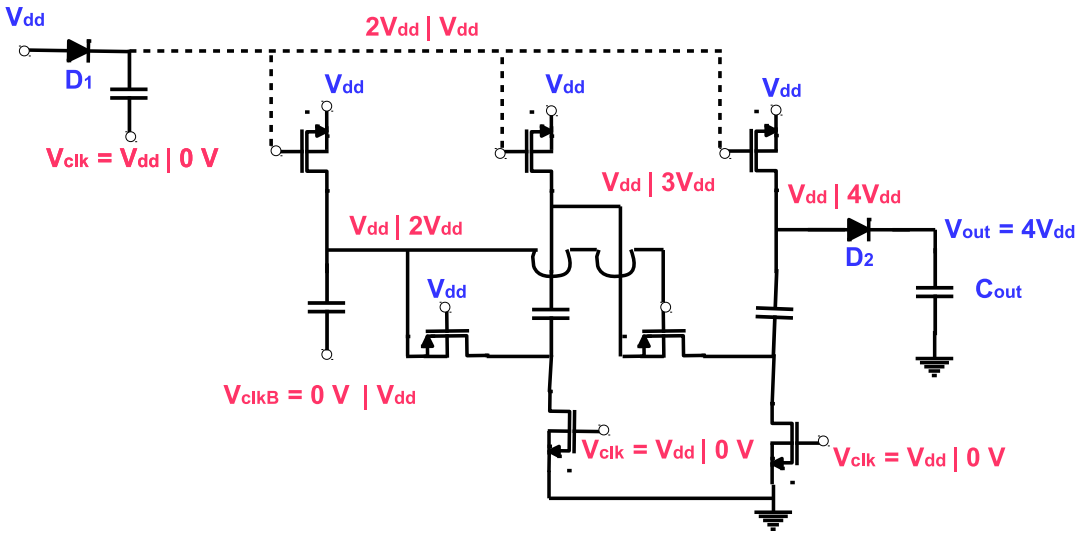



**Figure 4.3.:** Concept of the 3-stage proposed heap charge pump for high voltage generation [Reu13].

### 4.1.4 Proposed 4-phase Charge Pump Architectures for High Voltage Generation

Energy loss in charge pump circuits is normally divided in [MB13]:

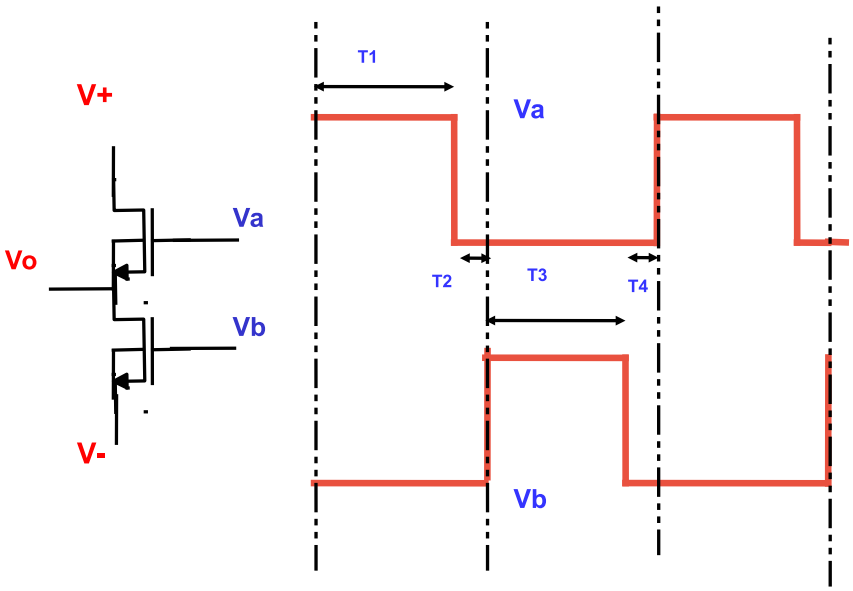
- **Redistribution loss:** The charge redistribution between capacitors can usually not be lossless, since pumping capacitors can only be charged in limited time and hence hardly be 100 % fully charged [WS11]. Optimized voltage conversion ratios can reduce this energy loss [KST05].
- **Switching loss:** It depends mainly on the clock frequency and parasitics of switches, which is not considerably influenced by circuit architectures.
- **Conduction loss:** It is mostly determined by the characteristics of devices. Different devices have different electrical characteristics, which should be considered when choosing circuit architectures. For example, Dickson charge pump using diodes has always about 0.7 $V$ voltage drop at each stage, while other charge pump architectures using MOS switches have much lower voltage drops. For the same type of devices such as MOS switches, lower on-resistance indicates lower conduction loss. Besides, the body effect of MOS switches can not be neglected.
- **Reversion loss:** It is mainly due to non-ideal control signals at MOS switches, so that a conduction path occurs at the clock switching time, when charge flows back from the higher stages to lower stages. Using ideal control signals, non-ideal switches with parasitic gate capacitors can be still hardly switched on and off immediately. Reversion loss decreases the voltage gain and power efficiency of the circuit.

In order to achieve the highest possible voltage gain (first of all, lowest possible conduction loss) and most compact possible chip area, Dickson charge pump architecture is excluded because of the

considerable voltage drop of its diodes or diode-connected MOSFETs. Pelliconi charge pump shows better voltage performance and provides less output voltage ripple. The charge transfer to the load at Pelliconi charge pump takes place during both halves of the clock period, whereas Dickson charge pump is only connected to the load during each second half of the clock period. However, the body effect and reverse current problems (reversion loss) limit its application in high voltage generation.

Therefore, the dynamic bulk-biasing technique [Shi+00] should be adopted to reduce the output voltage saturation caused by body effect of MOS switches and to avoid damages of MOS switches from the large current through their parasitic body diodes. The dynamic bulk-biasing technique is usually applied in PMOS transistors, where Bulk terminals are biased to the corresponding lowest or highest voltage level in the same charge pump stage. Because in CMOS bulk processes, NMOS transistors share usually the same p-substrate as their Bulk terminals, whose voltage level should normally always be the lowest potential in the whole circuit. Therefore, for NMOS transistors, this technique is only possible in triple-well processes, where Bulk terminals can be controlled by biasing techniques.

Dead time techniques [WTK10] can reduce reverse currents by forcing all the MOS switches open at the clock switching time, where the duration of all the open switches depends on the corresponding dead time. Dead time techniques can avoid circuit failure or undesired situations during the operation of circuits, for instance, the short-circuit caused by the conduction of two switches at the same time shown in Figure 4.4. During the dead time $T_2$ and $T_4$, there are supposed to be no events taking place. Moreover, dead times need to be reasonably short to avoid disturbing the normal operation phases of the circuit such as $T_1$ and $T_3$ in Figure 4.4. The feasibility to generate the required duration of dead times should be considered.




a) NMOS inverter b) 2-phase clock scheme with dead times

**Figure 4.4.:** Dead time application in NMOS inverter.

Introducing the discussed dynamic bulk-biasing and dead time techniques, a novel 4-phase charge pump architecture based on Pelliconi charge pump shown in Figure 4.5 is proposed for high voltage generation, which overcomes the drawbacks of Pelliconi charge pump such as the body effect and

reverse current problems, and provides higher voltage gain and power efficiency. Instead of using body biasing transistors for each MOS switches like in [Shi+00], the NMOS switches $M_1$ and $M_2$ responsible for the charge transfer at the same stage share the same couple of small extra NMOS transistors $M_5$ and $M_6$. $M_5$ and $M_6$ bias the connected Bulk terminals of all the NMOS transistors dynamically to the lower voltage level between Node $A$ and $B$, which are changeably to be the lowest voltage level at the current stage during each half clock period. The same case is applied to all the PMOS transistors $M_3$, $M_4$, $M_7$, $M_8$, $M_9$ and $M_{10}$, where the two small extra PMOS transistors $M_7$ and $M_8$ realize the dynamic bulk-biasing. The connected Bulk terminals of all the PMOS transistors are biased through $M_7$ and $M_8$ to the higher voltage level between Node A and B. The large pumping capacitors $C_1$ and $C_2$ are responsible for the charge transfer and provide the necessary voltage level to bias the Bulk terminals of all the NMOS switches. The small control capacitors $C_3$ and $C_4$ are used to control the PMOS charge transfer switches $M_3$ and $M_4$. The voltage levels at $C_3$ and $C_4$, namely Node $C$ and $D$, will be charged up to the same voltage level as those of $C_1$ and $C_2$ through the small PMOS switches $M_9$ and $M_{10}$ depending on the applied clock schemes. The additional PMOS control transistors $M_9$ and $M_{10}$ and capacitors $C_3$ and $C_4$ are intended for control signals. Therefore, their layout sizes are usually negligible. Compared with the large pumping capacitors $C_1$ and $C_2$; $C_3$ and $C_4$ can be charged and discharged faster, which indicates more effective control signals.

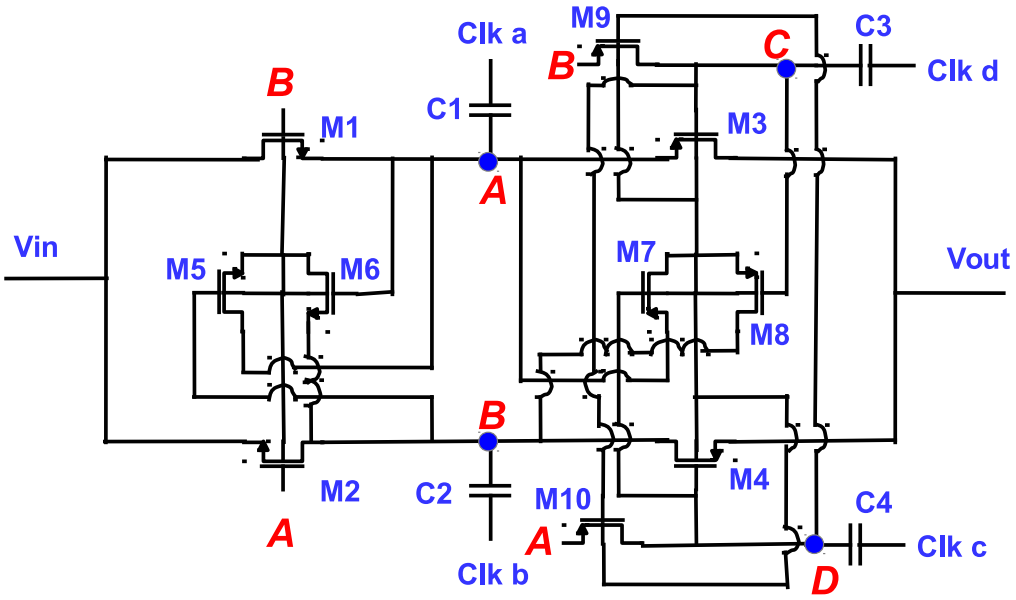



**Figure 4.5.:** Proposed 4-phase charge pump architecture employing dynamic bulk-biasing techniques.

Figure 4.6 shows the proposed 4-phase clock scheme to minimize reverse currents through the introduction of the short dead times $T_2$ and $T_4$ between the switching of the switches. During $T_2$ and $T_4$ or between the charge transfer phase $T_1$ and $T_3$, all the switches are forced to be shortly open, so that the possible cases for reverse currents between cascaded stages shown in Figure 4.7 can be avoided. The small control capacitors $C_3$ and $C_4$ are charged up by the large pumping capacitors $C_1$ and $C_2$ through small PMOS switches $M_9$ and $M_{10}$ during the charge transfer phases $T_1$ and $T_3$. The control signals at Node A,B,C and D can then always remain at the same voltage level. Other 4-phase charge pump architectures have been previously described in literatures. For example, in [WTK10], a 4-phase charge pump structure was proposed for low voltage applications without considering the body effect problems. However, its small control capacitors are connected to the corresponding large pumping capacitors during dead times, at which the voltage levels of large pumping capacitors

are low, while the voltage levels of small control capacitors are high. The proposed 4-phase charge pump architecture in this work for the high voltage generation can not only overcome the body effect and reverse current problem but also ensure that the small control capacitors are charged up correctly and no discharging will occur. Discharging of the pumping capacitors is stopped due to the disconnection with each other during the dead times. Figure 4.8 demonstrates the charge transfer in the proposed 4-phase charge pump. With multistage proposed charge pump, high output voltage can be generated.

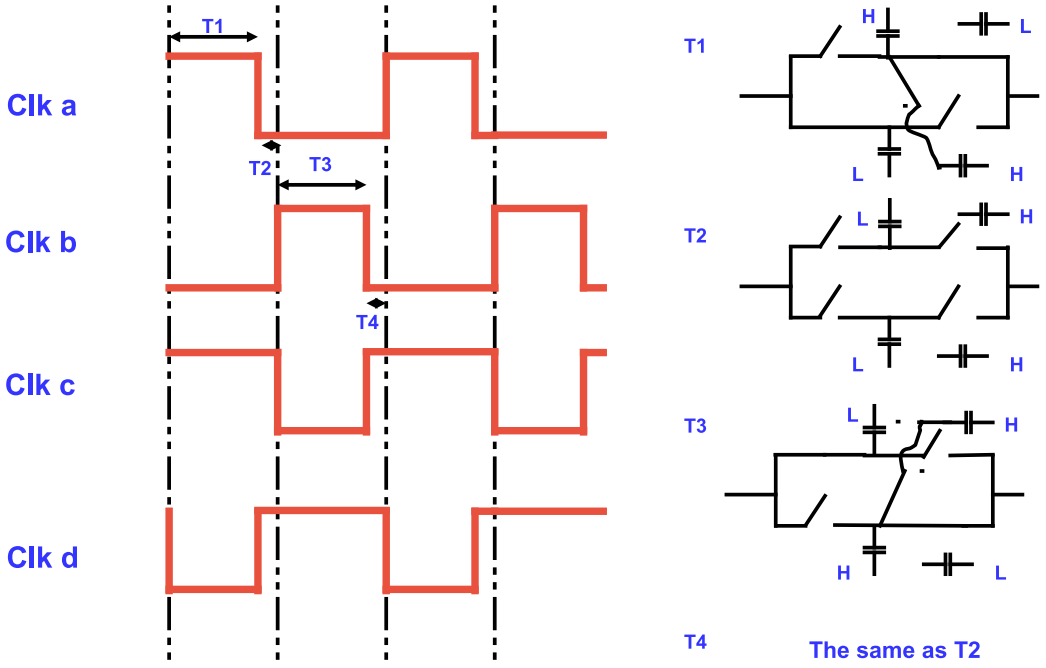



**Figure 4.6.:** Proposed 4-phase clock scheme with dead time techniques.

As a typical high voltage CMOS technology providing maximum operating voltages up to $120\,V$, the $0.35\,\mu m$ H35 of AMS was chosen to verify the proposed 4-phase charge pump architecture. With the knowledge about high voltage and isolated low voltage devices discussed in Section 2.2, the isolated low voltage CMOS transistors with $V_{GSmax} = 5.5\,V$, $V_{DSmax} = 5.5\,V$ and high voltage offset up to $120\,V$ at each terminal to the p-substrate were adopted to realize the PMOS and NMOS switches shown in Figure 4.5. At the clock switching time, two stacked switches, for example, the NMOS switch $M_1$ at the current stage and the PMOS switch $M_4$ at the former stage will experience a maximum $2V_{clk}$ short-time voltage spike. Assuming $V_{clk} = V_{dd}$, the DC power supply $V_{dd}$ should be kept below the $V_{DSmax}$ of the isolated devices, namely $5.5\,V$, to maintain the reliability. Otherwise, these isolated low voltage devices will be damaged. If the stage voltage gain is below $5.5\,V$ and the output voltage of the charge pump is below $120\,V$, then those isolated low voltage transistors with high voltage offset will always remain under their maximum allowed operating conditions. The deep NWELLs of isolated devices are not allowed to be floating and need to be biased to reasonable voltage levels to avoid the forward conduction and reverse breakdown of the high voltage pn-junctions between the deep NWELL and p-substrate and the low voltage pn-junctions inside each deep NWELL. High voltage transistors are not suitable for the proposed charge pump architecture due to their tied Bulk and Source terminals to avoid the latch-up and to reduce the body effect. In charge pumps, voltage levels at each side of MOS switches will be high and low alternatively, which leads

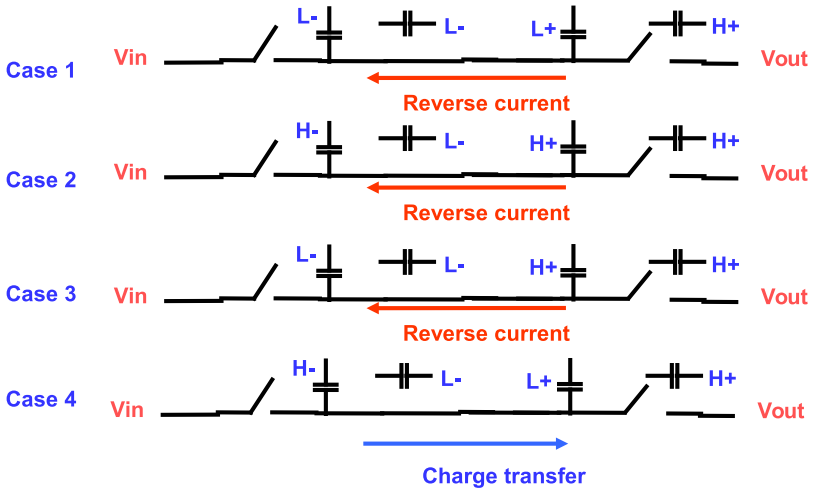



**Figure 4.7.:** Reverse currents in cascaded charge pump stages.

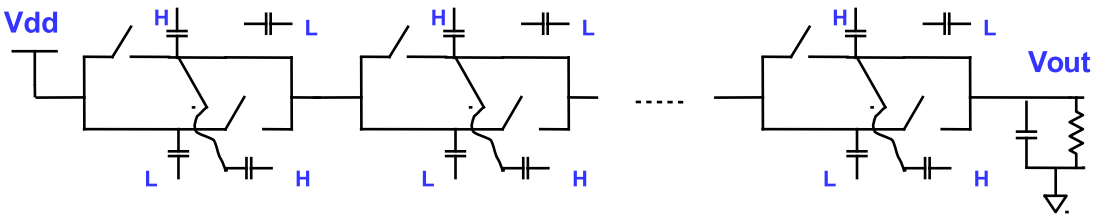



**Figure 4.8.:** Charge transfer in cascaded proposed 4-phase charge pump.

to the conduction of parasitic body diodes of MOS switches with tied Bulk and Source terminals during the second half clock period. Besides, their large layout sizes also constrict their applications in circuits of a high number of high voltage devices. The benefits of using low voltage isolated transistors are diminished layout area and conduction loss, increased switching speed and more stable electrical performance. Low voltage devices show significantly less degradation and life time reduction caused by voltage stresses under maximum allowed operating conditions compared with high voltage devices [Dat14c; Dat14b; Dat14g; Dat14f].

There are two types of high voltage sandwich capacitors, CWPM with $V_{max} = 70\,V$ and CPM with $V_{max} = 120\,V$ available in H35 (see Figure 2.9). The capacitance density of CWPM is almost twice of that of CPM. Therefore, to achieve the same capacitance, CWPM requires usually much smaller layout area. Both of them can be put on the deep NWELL, which provides a maximum $120\,V$ operating voltage between each terminal and the p-substrate. These high voltage sandwich capacitors have considerably large parasitics and occupy large chip area. However, they are the only choice for integrated high voltage capacitors above $50\,V$ in this technology.

High voltage sandwich capacitors occupy large layout area because of their low capacitance density, and have high parasitic capacitors to the p-substrate. Due to mainly the unequal parasitic capacitors at bottom and top plates of high voltage sandwich capacitors, different ways of the connection of those high voltage capacitors to the circuit have then different impacts on the voltage gain and power efficiency. The introduction of the deep NWELL increases the difficulty to analyze the effect caused by those parasitic capacitors. The default configuration of the high voltage sandwich capacitor CWPM is that the terminal composed of Metal 1 and Metal 3 layers is connected to the deep NWELL underneath the device, which is not recommended to be changed. The similar situation exists at the sandwich capacitor CPM. To simplify the discussion, two main configurations of high voltage sandwich capacitors are defined as following:

- **Config.1:** The deep NWELL is connected with one terminal of the high voltage capacitor in the charge pump and the clock drivers.
- **Config.2:** The deep NWELL is connected with one terminal of the high voltage capacitor in the charge pump, but not with the clock drivers.

It is evident that external clock drivers need to charge and discharge the large deep NWELL, if **Config.1** of high voltage sandwich capacitors is applied. This sacrifices the power efficiency due to the wasted charge. However, it maintains the stage voltage gain, because the parasitic capacitor at the other terminal is much less than that at the terminal connected with the deep NWELL. If **Config.2** is applied, the charge pump circuit must charge and discharge the large deep NWELL by itself, which leads to a significant reduction of the stage voltage gain. However, by using **Config.2**, less charge is wasted during the charging and discharging of the smaller parasitic capacitor at the other terminal by clock drivers, so that the power efficiency of the charge pump will be slightly improved compared with **Config.1**.

To illustrate the proposed 4-phase charge pump shown in Figure 4.5, schematic simulation results of a 2-stage charge pump can be found in Figure 4.9, where $C_1 = C_2 = 10\,pF$, $C_3 = C_4 = 313\,fF$, $C_L = 30\,pF$, clock frequency $f = 10\,MHz$, no load resistors, dead time $T_2 = T_4 = 8\,ns$ and $V_{clk} = V_{dd} = 3.7\,V$. All the capacitors are of the defined connection of **Config.1**. The input and output voltage of the second stage of the circuit are $7.36\,V$ and $11.004\,V$, respectively. The voltage at $C_1$, $C_2$, $C_3$ and $C_4$ are represented by the signals $V_{C1}$, $V_{C2}$, $V_{C3}$ and $V_{C4}$. It can be seen that the capacitors $C_1$, $C_2$, $C_3$ and $C_4$ are correctly charged up to the necessary control voltage level by the proposed 4-phase clock scheme shown in Figure 4.6. The Bulk terminals of the PMOS or NMOS switches are dynamically biased to the highest or lowest voltage level at the second stage during the charge transfer phase $T_1$ and $T_3$. Furthermore, due to the symmetrical structure of the isolated low voltage transistors with changeable Drain and Source terminals, the voltage difference $V_{sb}$ between Source

and Bulk terminals is zero, which resulting in the lowest threshold voltage, when the MOS switches are closed. $V_{sb}$ equals the highest stage voltage difference, which correspondingly resulting in very high threshold voltage, when the MOS switches are open. This helps significantly the reduction of the conduction loss and leakage current of the MOS switches. During the short dead time $T_2$ and $T_4$, when all the MOS switches are open, the Bulk terminals of the transistors are floating. At the same time, their voltage levels remain the highest or lowest voltage level at the current stage during the dead times. Therefore, the body effect problem is successfully solved and the conduction of body diodes in MOS switches is avoided, which indicates improved voltage gain and reliability. Using the same parameters and a load resistor of $R_L = 1.05\,M\Omega$, a 36-stage proposed 4-phase charge pump with capacitors of **Config.1** was simulated to demonstrate the reduction of the reverse current problem in Pelliconi charge pump. Figure 4.10 visualizes this improvement by comparing the reverse currents (positive values) at the output of the second stage of 36-stage Pelliconi charge pump (solid line, $I_{peak} = 1.035\,mA$ ) and the proposed 4-phase charge pump (dashed line, $I_{peak} = 20.788\,\mu A$), respectively.

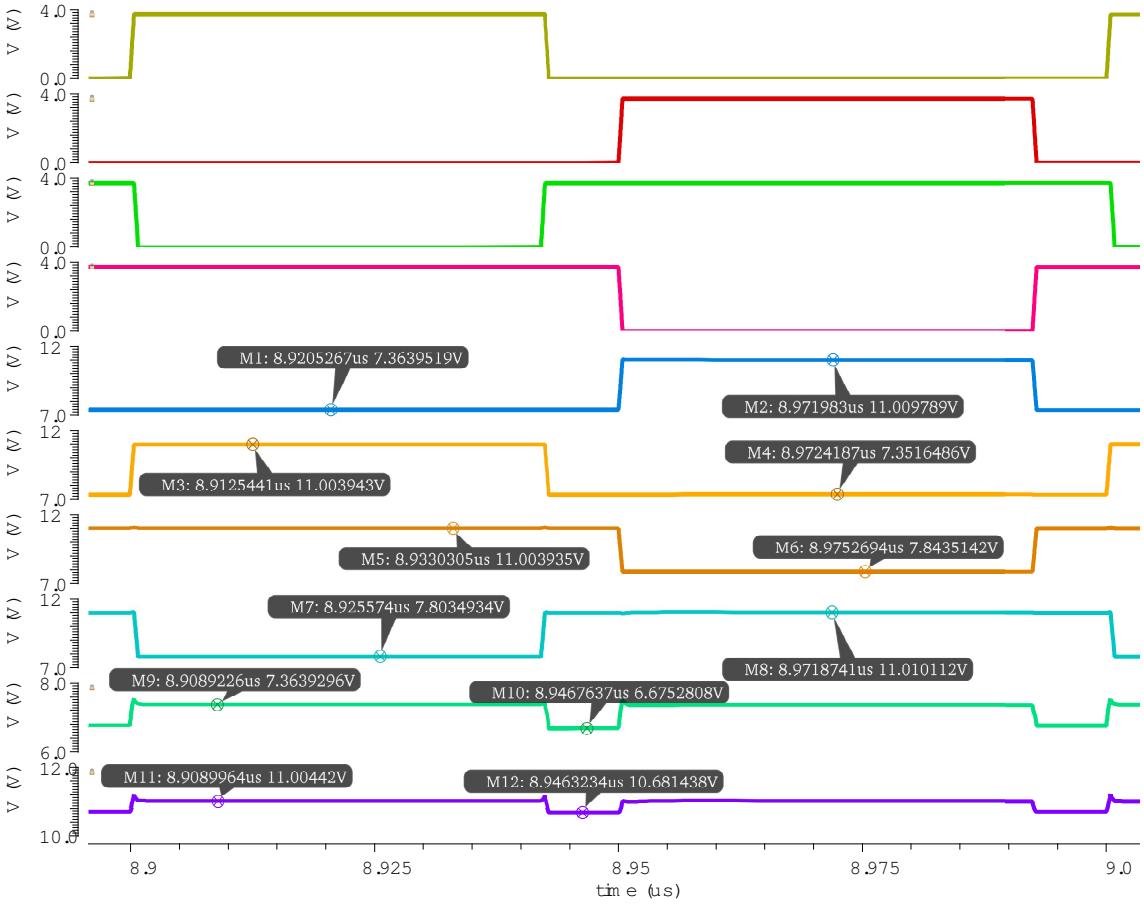



**Figure 4.9.:** Schematic simulation results at the second stage of a 2-stage proposed 4-phase charge pump (signals from top to bottom: CLKa, CLKb, ClKd, ClKc, VC2, VC1, VC4, VC3, VBulk(NMOSs), VBulk(PMOSs)).

Considering the impacts of **Config.1** and **Config.2** of high voltage sandwich capacitors, further simulations were performed. Table 4.1 explains the difference between **Config.1** and **Config.2** at various charge pump circuits regarding voltage gain and power efficiency. Charge pump circuits with high voltage sandwich capacitors of **Config.1** provide higher output voltages but suffer from lower power efficiency due to the wasted charge at the deep NWELL inside the capacitors (the large parasitic capacitor between the deep NWELL and p-substrate). Charge pump circuits with high voltage

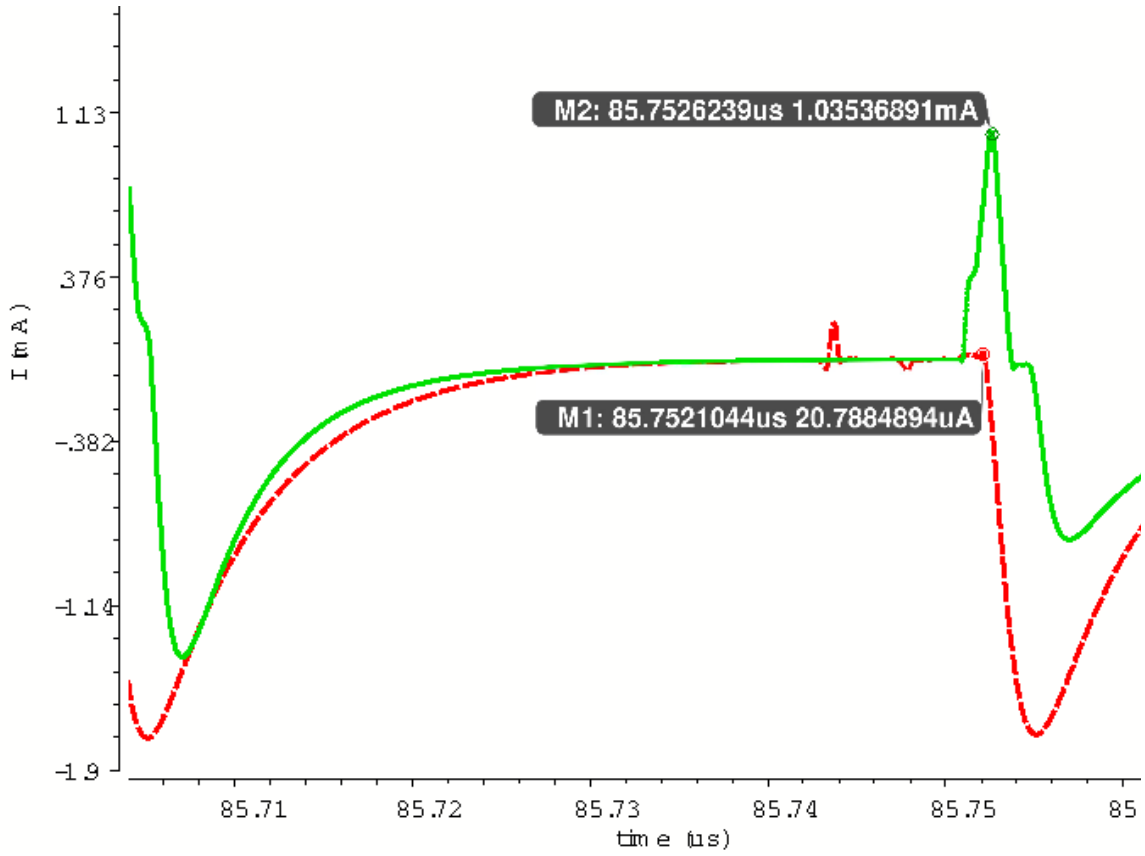



**Figure 4.10.:** Reverse current comparison.

sandwich capacitors of **Config.2** can generate lower output voltages because of the reduced effective pumping capacitor value caused by the large parasitic capacitors at the deep NWELL, although they avoid the meaningless charge and discharge of those large parasitic capacitors between the deep NWELL and the p-substrate by clock drivers. Lower output voltage or lower stage voltage gain means that less amount of charge is transferred from previous stages to next stages during each switching period. It should be pointed out that to achieve the same level of output voltages, circuits with capacitors of **Config.2** take much longer time under the same conditions compared with those of **Config.1**. Circuits with capacitors of **Config.1** require higher current from the DC power supply because of the additional charge and discharge of the large parasitic capacitors at the deep NWELL. Since charge pumps are usually applied in low power applications with insignificant heating problems, and charge pumps with higher voltage gain are more beneficial with respect to more compact layout size or further monolithic integration in CMOS technologies, high voltage sandwich capacitors of **Config.1** are preferred.

| **36-stage Charge Pump Circuits** | $V_{out}(V)$ | **Efficiency($\eta$)** |
|---|---|---|
| Pelliconi charge pump with Config.1 | 90 | 13 % |
| Pelliconi charge pump with Config.2 | 84 | 26 % |
| Proposed charge pump with Config.1 | 116 | 21 % |
| Proposed charge pump with Config.2 | 105 | 39 % |

**Table 4.1.:** Simulation results of various 36-stage charge pumps.

The proposed 4-phase charge pump architecture shown in Figure 4.5 consists of NMOS and PMOS transistors as switch elements. Nevertheless, it is always desired to design the circuit with only one

type of transistors in order to simplify the layout design and to avoid the latch-up effect. Especially PMOS transistors are usually more popular, because they do not require special triple-well CMOS processes, although they show higher channel resistance than NMOS ones of the same dimension. By introduction of additional control capacitors, better control concepts of switches can be realized. Therefore, other 2 new 4-phase charge pump architectures extended from the previously proposed one can be obtained by small modifications.

Figure 4.11 displays a circuit architecture, in which merely PMOS transistors are applied. The PMOS switches $M_1$ and $M_2$ are directly controlled by the large pumping capacitors $C_1$ and $C_2$. This architecture suffers from the threshold voltage drop of PMOS switches $M_1$ and $M_2$, since these two transistors are both diode-connected similar to those in Dickson charge pump. Consequently, the stage voltage gain is reduced significantly because of the approximately $0.7\,V$ threshold voltage drop of the MOS switches $M_1$ and $M_2$, which is already not suitable for applications with low voltage DC power supplies.

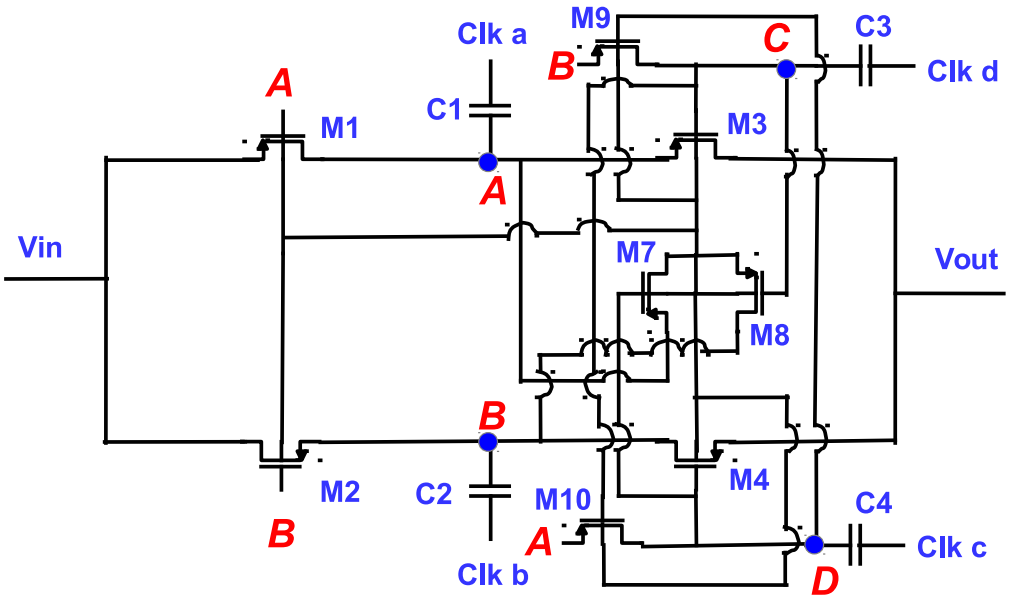



**Figure 4.11.:** Proposed 4-phase charge pump architecture with all PMOS transistors.

Figure 4.12 demonstrates a modified circuit of the proposed charge pump architecture, in which more precise control of the NMOS switches $M_1$ and $M_2$ is realized by using two additional small control capacitors $C_5$ and $C_6$. These two capacitors are charged up through two small PMOS transistors $M_{11}$ and $M_{12}$ to the same voltage level as those of the large pumping capacitors $C_1$ and $C_2$ at the same stage during the charge transfer phases $T_1$ and $T_3$, when the proposed 4-phase clock scheme in Figure 4.6 is applied. Compared to the large pumping capacitors $C_1$ and $C_2$, $C_5$ and $C_6$ can be charged and discharged faster, which indicates more effective control signals than those in the proposed charge pump architecture in Figure 4.5.

Schematic simulations for comparison among the 3 proposed 4-phase architectures were performed under the following conditions: $C_1 = C_2 = 10\,pF$, $C_3 = C_4 = C_5 = C_6 = 313\,fF$, $C_L = 30\,pF$, clock frequency $f = 10\,MHz$, $R_L = 1.0\,M\Omega$, dead time $T_2 = T_4 = 8\,ns$ and $V_{clk} = V_{dd} = 3.7\,V$. **Config.1** of the high voltage sandwich capacitors was chosen due to its better voltage gain. The power efficiency was calculated by the proportion between output power and input power of the circuit.

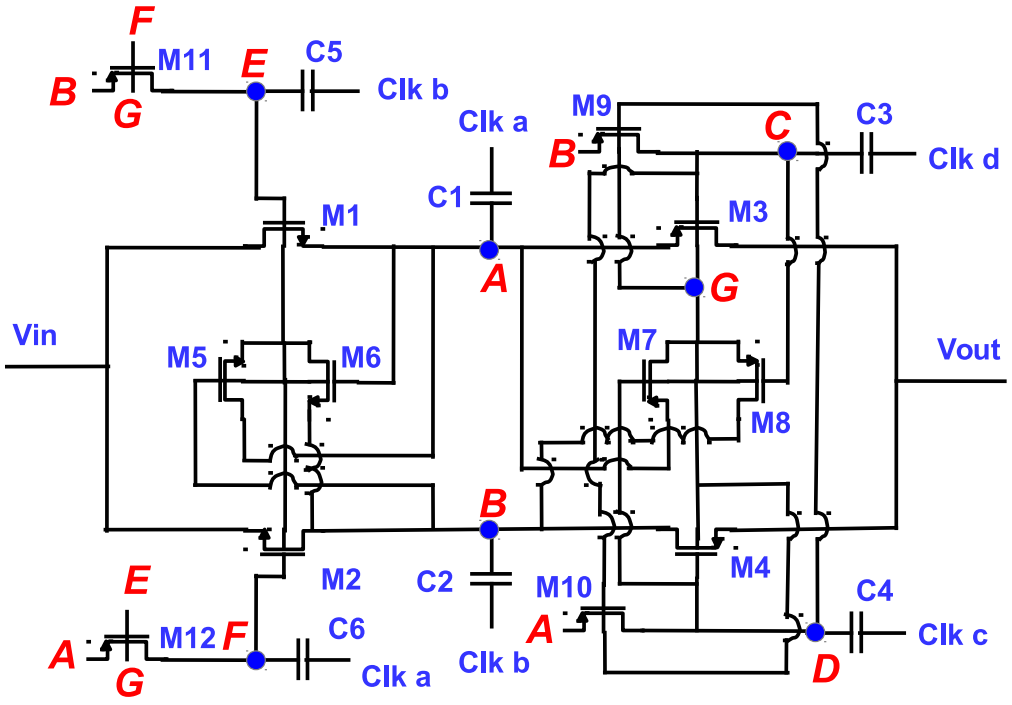



**Figure 4.12.:** Proposed 4-phase charge pump architecture with enhanced control circuits.

| 36-stage Charge Pump Circuits | $V_{out}(V)$ | Efficiency($\eta$) |
|---|---|---|
| Proposed 4-phase charge pump with all PMOS transistors (Config.1) | 72.5 | 8.9 % |
| Proposed 4-phase charge pump with enhanced control circuits (Config.1) | 115.9 | 19.6 % |
| Proposed 4-phase charge pump (Config.1) | 115.7 | 20.5 % |

**Table 4.2.:** Comparison of different proposed 4-phase charge pump architectures.

It has been proven in Table 4.2 that the architecture shown in Figure 4.11 using only PMOS switches can generate rather lower output voltage of 72.5 $V$. In contrast, the other two architectures have much higher output voltages of approximately 115 $V$. Although the architecture in Figure 4.12 with enhanced control circuits can provide slightly higher output voltages, it consumes correspondingly more power. Hence, it has lower power efficiency compared to the previously proposed one in Figure 4.5 because of its additional control circuits. Furthermore, it occupies also larger layout area due to its additional capacitors and transistors. To save the chip area and power consumption, the previously proposed architecture in Figure 4.5 is more suitable for the monolithic integration of charge pump circuits in high voltage applications. Besides, all the proposed 4-phase architectures benefit from the dynamic bulk-biasing technique to overcome the body effect problem, and can reduce the reversion loss between cascaded stages. The SOAC ensuring that all the devices operate always under their maximum allowed operating conditions, which is discussed in Section 3.1.1, was taken into account during all the simulations. Hence, the robustness and reliability of the proposed 4-phase architectures were proven by design kits in EDA tools.

### 4.1.5 Influences of High Voltage Capacitors on Voltage Gain and Power Efficiency

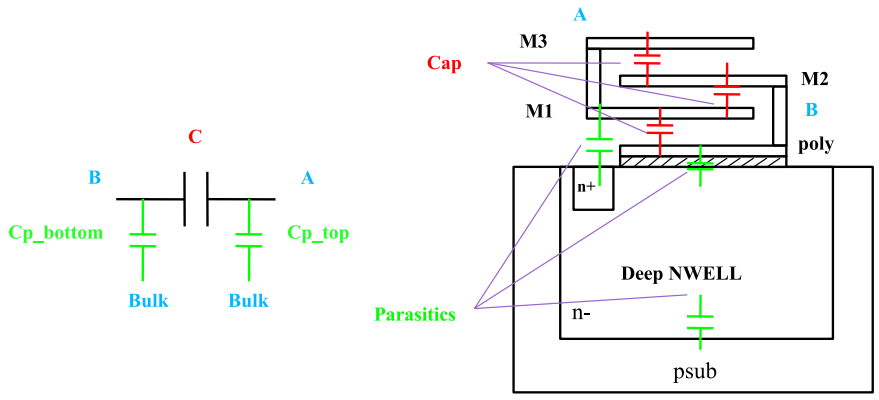
In Section 2.2, it is already mentioned that high voltage sandwich capacitors in current CMOS technologies have large parasitic capacitors, which have significant impacts on the performance of the whole circuit. With the introduced deep NWELL for high voltage offset to the p-substrate, the analysis of the effects caused by those parasitic capacitors becomes difficult. In Section 4.1.4, two configurations of high voltage sandwich capacitors are defined, namely **Config.1** and **Config.2**. To explain this phenomenon, several post-layout simulations were performed. All the post-layout simulations using the high voltage CMOS technology H35 of AMS are based on the proposed 4-phase charge pump architecture in Figure 4.5. The parameters for the simulations were identical to those adopted for the simulation results in Table 4.1. It can be seen from the post-layout simulation results of various multistage circuits using the proposed 4-phase charge pump architecture in Table 4.3, that the circuit with all capacitors of **Config.1** has higher stage voltage gain but lower power efficiency compared with the circuits with all capacitors of **Config.2**. In order to achieve the same output voltage level, circuits with all capacitors of **Config.2** must have higher stage number, which leads to larger layout size. Although circuits with all capacitors of **Config.2** can save the power even with higher stage number, circuits with all capacitors of **Config.1** are more reasonable regarding levels of integration in low power applications.

Comparison of the post-layout simulation results in Table 4.3 with the schematic simulation results in Table 4.1 shows the importance of accuracy of the device models. During the post-layout simulation, all the necessary parasitic capacitors and resistors were included, while those parasitic capacitors and resistors are missing or not modeled in device models of high voltage sandwich capacitors during the schematic simulation. Hence, post-layout simulations are more meaningful, when the design includes devices with large parasitics such as high voltage sandwich capacitors.

| **Charge Pump Circuits** | **Stage Number($n$)** | $V_{out}(V)$ | **Efficiency($\eta$)** |
|---|---|---|---|
| Proposed 4-phase charge pump with all capacitors of Config.1 | 36 | 112.44 | 12.7 % |
| Proposed 4-phase charge pump with all capacitors of Config.2 | 36 | 102.8 | 17.5 % |
| Proposed 4-phase charge pump with all capacitors of Config.2 | 40 | 112.45 | 19.2 % |

**Table 4.3.:** Post-layout simulation results of various multistage proposed 4-phase charge pump.

**Config.1** and **Config.2** of high voltage sandwich capacitors are mainly related to the available high voltage sandwich capacitor CWPM with $V_{max} = 70\,V$ in the high voltage CMOS technology H35 of AMS. Its terminal composed of Metal 1 and Metal 3 is connected to the deep NWELL underneath the device by default. This configuration is not suggested to be changed by the foundry AMS. The other high voltage sandwich capacitor CPM with $V_{max} = 120\,V$ can be configured like CWPM, so that **Config.1** and **Config.2** can also be applied to it. Nevertheless, the deep NWELL is not a necessary part of CPM. Even if the deep NWELL exists at CPM, the deep NWELL can be biased by different ways. In Figure 4.13, the generic simulation model of high voltage sandwich capacitors is illustrated, in which only considerable parasitic capacitors are included. The nominal capacitance $C$ is composed of the capacitors between Metal 3 and Metal 2, Metal 2 and Metal 1, and Metal 1 and polysilicon layers. The parasitic capacitors between top metal plates to the bulk are negligible when compared to those between bottom polysilicon layer and the bulk. The bulk can be either the p-substrate or deep NWELL in the p-substrate. The deep NWELL is frequently applied to increase the vertical high voltage performance of devices, namely to provide high voltage offset at each terminal to the p-substrate. However, the application of the deep NWELL causes the change of parasitic capacitors at those high voltage sandwich capacitors.




a) Device model b) Cross section including parasitics

**Figure 4.13.:** Generic model of high voltage sandwich capacitors.

The deep NWELL beneath the device is not allowed to be floating for avoiding hot-nwell problems [3]. In order to investigate the influences caused by the deep NWELL, three typical configurations of sandwich capacitors regarding the deep NWELL are defined:

- **Config.a**: Device lies directly on p-substrate without the deep NWELL.
- **Config.b**: Device lies on the deep NWELL biased by the available DC power supply.
- **Config.c**: Device lies on the deep NWELL biased by Terminal B of the device.

These three configurations of high voltage sandwich capacitors, or more exactly, of CPM, have different impacts on voltage gain and power efficiency of charge pump circuits than **Config.1** and

[3] Hot-nwell problems will be reported after the DRC in EDA tools, if NWELL is floating, which leads to unreliable performance of the device.

**Config.2**. **Config.1** and **Config.2** discuss mainly the influence of the large parasitic capacitor between the deep NWELL and the p-substrate, since the deep NWELL is already connected with one terminal of the device in those 2 configurations. **Config.a**, **Config.b** and **Config.c** focus mainly on the effective overall capacitance of different parasitic capacitors. The comparison between **Config.a**, **Config.b** and **Config.c** can be demonstrated in Table 4.4 by the post-layout simulation results of 4-stage charge pump circuits based on the proposed 4-phase charge pump architecture in Figure 4.5. Considering the importance of voltage gain, Terminal B of capacitors is connected to clock drivers in all the post-layout simulations. If Terminal B of sandwich capacitors with large bottom parasitic capacitors is connected with clock drivers, the power loss by unnecessary charge und discharge of those bottom parasitic capacitors will be substantial, but the effective pumping capacitor value related to stage voltage gain will not be affected seriously by the small parasitic capacitors at the top plates. On the contrary, when Terminal B of sandwich capacitors is connected directly to the charge pump, the effective pumping capacitor value will be decreased heavily, which is not desired to achieve high voltage gain.

| Charge Pump Circuits | Output Voltage | Power Consumption |
|---|---|---|
| Proposed 4-phase charge pump (Config.a) | low | medium |
| Proposed 4-phase charge pump (Config.b) | medium | high |
| Proposed 4-phase charge pump (Config.c) | high | low |

**Table 4.4.:** Comparison among different configurations of high voltage sandwich capacitors.

As shown in Table 4.4, **Config.c** can provide the best power efficiency, because under the same operating conditions, the parasitic capacitors between the deep NWELL and p-substrate are smaller than those between polysilicon layer and p-substrate in **Config.a**. The capacitance density between the deep NWELL and p-substrate is lower than that between the polysilicon layer and p-substrate. More charge is wasted in **Config.a** compared with **Config.c** due to unnecessary charge and discharge of the corresponding bottom parasitic capacitors by clock buffers. **Config.b** shows the worst power efficiency mainly due to the large parasitic capacitor between the polysilicon layer and deep NWELL similar to that in **Config.a** and the additional leakage current from the DC supply through the deep NWELL to the p-substrate. If the deep NWELL is biased by the DC power supply with stable voltage levels, they are similar to those connected with the p-substrate, when the bottom parasitic capacitors are calculated.

The high stage voltage gain in **Config.c** can be explained by the negligible parasitic capacitance at top metal layers Metal 1 and Metal 3, which will not change the effective pumping capacitance value significantly. Moreover, the parasitic capacitors between top metal layers Metal 1 and Metal 3 and the deep NWELL become a part of the effective pumping capacitor value, which increases the total effective pumping capacitance and the stage voltage gain. In **Config.b**, the deep NWELL is biased by the DC power supply with stable voltage levels, which are higher than that of the p-substrate. Therefore, less charge is wasted through charge and discharge of the parasitic capacitors between top metal layers and the biased deep NWELL than in **Config.a** directly between top metal layers and the p-substrate. Under the same operating conditions, the effective pumping capacitor value at **Config.c** is hence the highest among the discussed three configurations. **Config.b** provides the second highest effective pumping capacitor value. **Config.a** shows however the lowest one. It is proven that it is of advantage to bias the deep NWELL directly with one terminal of the device such as Terminal B in order to reduce the effect caused by parasitic capacitors[4]. Nevertheless, in applications where high voltage sandwich capacitors are not used as pumping capacitors and Terminal B of sandwich capacitors are biased at stable voltage levels instead of being driven by clock drivers, these three configurations do not show much difference.

[4] Similar conclusion can be concluded, when Terminal A of the device is shorted with the deep NWELL.

### 4.1.6 Comparison and Discussion

Dickson charge pump and heap charge pump are both not suitable as integrated high voltage generators, since the voltage drop of diodes or diode-connected MOSFETs in Dickson charge pump is considerably large and the parasitic capacitors of the pumping capacitors in heap charge pump decrease the voltage gain seriously . Pelliconi charge pump using isolated low voltage transistors can be easily applied in integrated circuits and provide higher voltage gain. However, Pelliconi charge pump suffers from the body effect problem of MOS switches and the reverse current problem between cascaded stages, which result in reduced output voltages. The proposed 4-phase charge pump architecture in Figure 4.5 shows significantly improved voltage gain and power efficiency mainly due to the reduction of the reverse currents and the overcome of the body effect problem in comparison with Pelliconi charge pump. The other proposed 4-phase charge pump architectures in Figure 4.11 and 4.12 show lower voltage gain or require larger layout size compared with the proposed 4-phase charge pump architecture in Figure 4.5. Therefore, the proposed 4-phase charge pump architecture in Figure 4.5 is the most suitable architecture among all the discussed charge pump architectures with respect to voltage gain, layout area, power efficiency etc.

An advanced 4-phase clock scheme with dead time techniques in Figure 4.6 is adopted to reduce reverse currents, which is intended to be employed in the proposed 4-phase charge pump architecture in Figure 4.5. Influences of the dead time duration on the output voltage ripple should be taken into account, because during the dead time the load capacitor $C_L$ is disconnected with the charge pump and therefore the output voltage $V_{out}$ will be decreased by load currents. The output voltage drop during the dead time (not the overall output voltage ripple) can be calculated by Equation 4.6. Shorter dead times ensure a more stable output voltage with lower voltage ripple. However, too short dead times will be a huge challenge for the clock generation and distribution.

$$V_{ripple(deadtime)} = \frac{I_L T_{deadtime}}{C_L} \tag{4.6}$$

Different configurations of pumping capacitors also have influences on the voltage gain and power efficiency of the charge pump. For higher voltage gain, **Config.1** of high voltage sandwich capacitors defined in Section 4.1.4 is more appropriate but with lowered power efficiency. **Config.2** also defined in Section 4.1.4 is able to increase the power efficiency. However, it has lower voltage gain, which requires more stages (larger layout size) to achieve the similar output voltage compared with **Config.1**. In both **Config.1** and **Config.2**, the introduced deep NWELL underneath the high voltage sandwich capacitors is connected with one terminal of the capacitors. This configuration is related to the **Config.c** defined in Section 4.1.5, which shows highest voltage gain and lowest power efficiency in comparison to **Config.a** (no deep NWELL below high voltage capacitors) and **Config.b** (deep NWELL biased by DC power supply).

The capacitor values of the small control capacitors $C_3$ and $C_4$ in Figure 4.5 should be chosen carefully, especially during the post-layout simulation, so that they are not too large to affect the voltage gain significantly, because they also need to be charged by the large pumping capacitors $C_1$ and $C_2$. Nevertheless, too small values of $C_3$ and $C_4$ are not sufficient to control the MOS switches. In those cases with too small values of $C_3$ and $C_4$, parasitic capacitors will reduce the voltage levels at $C_3$ and $C_4$. It can result in unstable voltage levels at $C_3$ and $C_4$.

## 4.2 Fully Integrated High Voltage Charge Pump "Achilles"

In order to verify the proposed 4-phase charge pump architecture in Figure 4.5, a test chip is required. Using the 0.35 $\mu m$ high voltage CMOS technology H35 of AMS, a 36-stage fully integrated charge pump with capacitors of **Config.1** defined in Section 4.1.4 was designed. Parameters for

PMOS and NMOS switches are optimized with respect to voltage gain and power efficiency. Clock frequency of $10\,MHz$ is chosen due to its simplicity for the clock implementation and correspondingly smaller pumping capacitors. According to Equation 4.4, the pumping capacitors $C_1$ and $C_2$ in Figure 4.5 are chosen to be approximately $10\,pF$, respectively, while $C_3 = C_4 = 313\,fF$. To stabilize the output voltage, a $6\,pF$ high voltage sandwich capacitor CPM discussed in Section 4.1.5 is added at the output of the 36-stage charge pump. Some important schematic and post-layout simulation results of this 36-stage charge pump are already presented in Table 4.1 and 4.3.

### 4.2.1 Layout Implementation

To fulfill the high voltage design rules of H35, the approximately $10\,pF$ pumping capacitors $C_1$ and $C_2$ are implemented by an array of small unit capacitors to reduce mechanical stresses. High voltage sandwich capacitor CWPM with maximum allowed operating voltage up to $70\,V$ is adopted in the first 18 stages. And CPM with maximum allowed operating voltage up to $120\,V$ is adopted in the last 18 stages. In this way, the layout area can be optimized. The choice of the $313\,fF$ small control capacitors instead of even lower capacitor values is based on the consideration of parasitic capacitors of the high voltage sandwich capacitors. In Figure 4.14, a single stage layout of the designed 36-stage charge pump using CWPM as the pumping and control capacitors is demonstrated. It can be seen that including high voltage guard rings, the capacitors occupy the main part of the layout. The major current path is constructed by the thick and wide power metal layer (Metal 4) to avoid electromigration, in which small slots are introduced for the release of possible mechanical stresses. The deep NWELLs of all the MOSFETs in this single stage are located inside the same guard ring and are connected together to be biased at the same voltage level. The voltage difference of all the pn-junctions inside the deep NWELLs are kept within their safe operating areas. The layout size of this single stage is about $0.21\,mm^2$.

Furthermore, 4 low voltage huge clock drivers composed of tapered CMOS inverters for each phase of external clock signals are included on-chip to provide sufficient currents to the charge pump circuit, which are isolated from the high voltage blocks by guard rings. Adequate low voltage stabilizing capacitors are placed between power and ground lines to reduce input voltage ripples. Figure 4.15 demonstrates the chip layout of the designed 36-stage charge pump including clock drivers, power/ground and I/O pads with ESD protection structures. The layout size for the entire high voltage ASIC with codename "Achilles" amounts to $3.9 \times 5.6 = 21.84\,mm^2$, where the 36-stage charge pump alone occupies $3.2 \times 4.5 = 14.4\,mm^2$.

### 4.2.2 Measurement Results

The test chip with codename "Achilles" fabricated in AMS $0.35\,\mu m$ $120\,V$ CMOS technology H35 was received in late April in 2012 (see Figure 4.16). This high voltage ASIC was not packaged and needed to be mounted on an empty chip socket, whereby bond pads were bonded to the chip socket pins. All measurements were performed on a wafer prober with probe needles. External clock signals are generated by the signal generator to drive the clock buffers inside the chip.

This fully integrated test chip is able to generate up to $120\,V$ high DC output voltage from $3.7\,V$ low voltage DC power supply at approximately $1\,M\Omega$ load resistor and $10\,MHz$ external clock signals. The ramp-up time for the output voltage to reach $120\,V$ from $0\,V$ at $50\,pF$ load capacitor and approximately $1\,M\Omega$ load resistor is about $1\,ms$. The overall power efficiency of this test chip is about 14 %, which is still acceptable considering the $100\,mW$ average power consumption. The on-chip clock drivers consume considerable power, about 30 % of the total power consumption. At such low average power consumption, the surface temperature of this high voltage ASIC was measured by means of infrared camera after long time operation, which remained the room temperature. It indicates that no heat sink or other cooling methods are required.

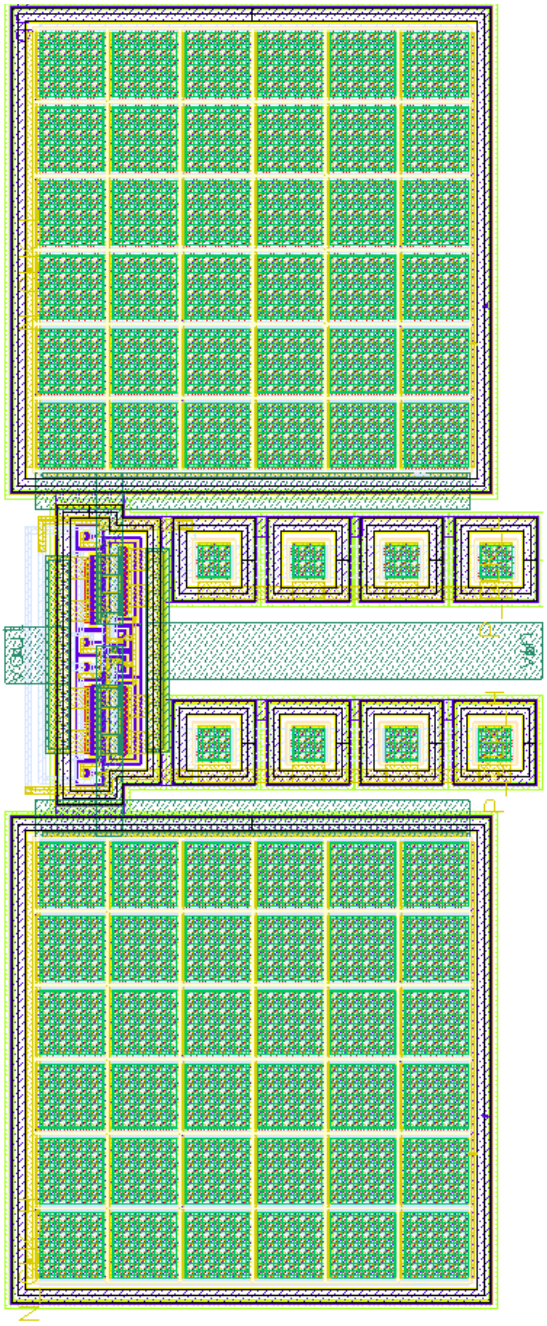


**Figure 4.14.:** Layout of a single stage proposed 4-phase charge pump using H35.

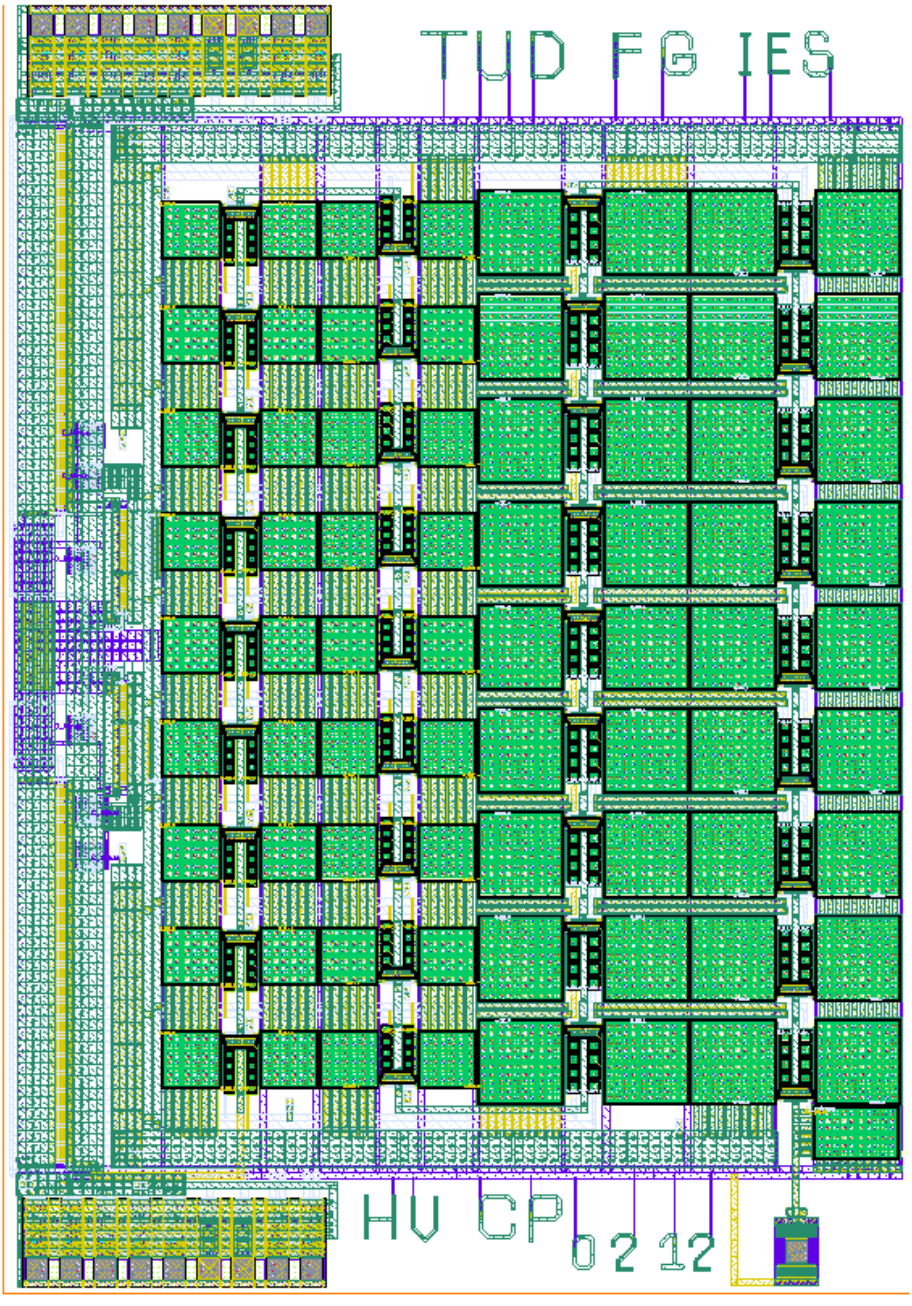



**Figure 4.15.:** Chip layout of the 36-stage proposed 4-phase charge pump "Achilles".

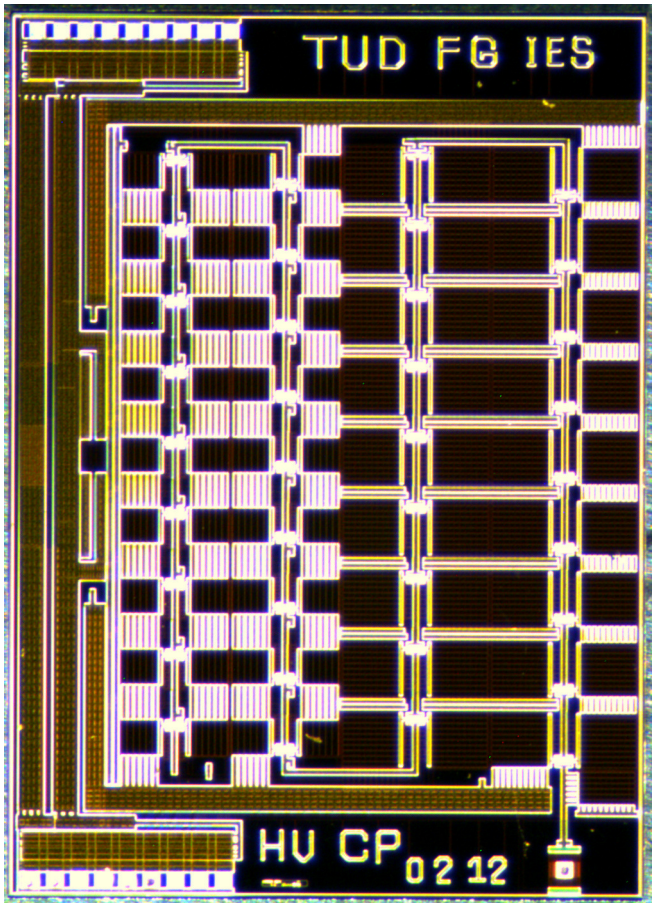



**Figure 4.16.:** Chip photograph of the 36-stage proposed 4-phase charge pump "Achilles".

To illustrate the reduction of reverse currents, some measurements by means of the conventional 2-phase non-overlapping clock scheme and the proposed 4-phase clock scheme shown in Figure 4.6 were performed. The 2-phase non-overlapping clock scheme can be easily achieved at the proposed 4-phase charge pump architecture by reducing the dead time $T_2$ and $T_4$ to $0\,ns$. In this case, the proposed charge pump circuit is similar to Pelliconi charge pump. For the proposed 4-phase clock scheme with dead times, $T_2$ and $T_4$ were set to $8\,ns$. The other measurement conditions were: clock frequency $f = 10\,MHz$, $V_{clk} = V_{dd} = 3.7\,V$, $C_L = 50\ pF$, $R_L = 910\,k\Omega$.

In Table 4.5 and 4.6, the benefits of the proposed 4-phase clock schemes compared with the 2-phase non-overlapping clock scheme are proven by the measurement results.

| **Clock Schemes** | $V_{out}(V)$ | $V_{dd}(V)$ | $I_{dd}(mA)$ |
|---|---|---|---|
| Non-overlapping 2-phase clock scheme | 104 | 3.3 | 20.055 |
| Proposed 4-phase clock scheme | 116 | 3.3 | 19.244 |

**Table 4.5.:** Comparison between 2-phase non-overlapping clock scheme and proposed 4-phase clock scheme without load resistors.

| **Clock Schemes** | $V_{out}(V)$ | $V_{dd}(V)$ | $I_{dd}(mA)$ | **Efficiency**($\eta$) |
|---|---|---|---|---|
| Non-overlapping 2-phase clock scheme | 96.7 | 3.7 | 25.97 | 10.69 % |
| Proposed 4-phase clock scheme | 111 | 3.7 | 25.30 | 14.46 % |

**Table 4.6.:** Comparison between 2-phase non-overlapping clock scheme and proposed 4-phase clock scheme with load resistor = 910 kOhm.

### 4.2.3 Comparison and Discussion

The proposed 4-phase charge pump architecture in Figure 4.5 from Section 4.1.4 was successfully implemented and verified in the test chip "Achilles". The benefits of the proposed 4-phase clock scheme with dead time techniques in Figure 4.6 compared with the 2-phase non-overlapping clock scheme was proven by the measurement results in Section 4.2.2.

Up to now, the on-chip high voltage generation relies mainly on integrated boost converters with external inductors. Conventional charge pump architectures such as Dickson charge pump, Pelliconi charge pump, heap charge pump etc. are frequently applied in integrated circuits. However, due to their drawbacks (see Section 4.1.1, 4.1.2 and 4.1.3), they are more suitable for low voltage applications. With the development of high voltage CMOS technologies, some charge pump architectures for high voltage generation were proposed but only by simulation results [Zl07; LS12]. In [EAS13], a fully integrated charge pump based on Cockcroft-Walton charge pump [PS06] was reported (see Table 4.7), which uses series capacitors for the charge transfer and is only able to provide low load currents ($< 10\,\mu A$), while "Achilles" can provide about $100\,\mu A$ at even higher output voltages. The fully integrated charge pump in [Dou10] also shown in Table 4.7 is basically Dickson charge pump, which adopted body diodes of DMOS as charge transfer elements. Its voltage gain is therefore limited and its output current is also low, about $50\,\mu A$. The comparison between the layout size, power efficiency, voltage gain is not easy, since "Achilles" and the high voltage charge pumps in [EAS13; Dou10] have adopted CMOS technologies of different feature sizes and different voltage levels of DC power supplies. However, "Achilles" shows much higher output voltage and voltage conversion

ratio, which still enables a monolithic solution for the on-chip high voltage generation using CMOS technologies. Therefore, "Achilles" is believed to be the first fully integrated charge pump using CMOS technologies, which is able to generate output voltages above $100\,V$ from low voltage DC power supplies such as $3.7\,V$ .

| **Reference** | **Max.** $V_{out}(V)$ | $V_{dd}(V)$ | $f_{clk}(MHz)$ | **Switch Type** | **Technology**($\mu m$) |
|---|---|---|---|---|---|
| [EAS13] | 51 | 6 | 0.5 | PMOS | 0.6 |
| [Dou10] | 55 | 3 | 10 | Body diode of DMOS | 0.7 |
| Achilles | 120 | 3.7 | 10 | CMOS | 0.35 |

**Table 4.7.:** Comparison between fully integrated high voltage charge pump in [EAS13], [Dou10] and "Achilles".

Due to the more significant parasitics in high voltage devices, post-layout simulation results show higher accuracy than those of the schematic simulation. The influences of clock frequencies and DC power supplies on the output voltage of the proposed 4-phase charge pump are analyzed in the second high voltage ASIC "Balios" in Section 4.3. It is obvious that with larger load resistors (lower load currents), the output voltage of "Achilles" will rise, and vice versa. By increasing the capacitor value of the load capacitor, the output voltage ripple can be reduced. However, the ramp-up time and recovery time of the circuit will become longer.

## 4.3 Fully Integrated High Voltage Charge Pump "Balios" with On-chip Clock Generation

The second chip received in August of 2013 with codename "Balios" was fabricated in the same CMOS technology H35 used by the first test chip "Achilles". It consists of 40-stage proposed 4-phase charge pump architecture shown in Figure 4.5, 4-phase on-chip clock generators and large clock buffers. Two identical 4-phase on-chip clock generators are implemented in "Balios". One is for the clock generation of "Balios". The other is for independent applications. The proposed 4-phase charge pump architecture was already verified and proven in "Achilles", so that only optimization of circuit parameters is necessary instead of modifications of circuit architectures. Therefore, there are no probe pads designed in the "Balios" packaged with JLCC84.

Since the clock frequency of the charge pump is increased to $20\,MHz$ in "Balios", the pumping capacitors at each stage are reduced to totally approximately $10\,pF$ at each stage (at "Achilles" totally $20\,pF$), which results in a reduced charge pump area of $2.3 \times 4 = 9.2\,mm^2$. The entire chip size including two identical on-chip 4-phase clock generators and clock drivers amounts to $4.4 \times 4 = 17.6\,mm^2$. The output voltage of "Balios" is slightly higher than that of "Achilles" at same operating conditions due to its higher stage number. However, the power consumption and power efficiency of "Balios" are lower because of the additional circuits for the clock generation.

### 4.3.1 On-chip Clock Generation

Traditional ring oscillators are not able to provide constant clock frequencies at PVT variations. The tolerance of the clock frequency can be even about 20 % of the designed frequency. In [SAA06], a $7\,MHz$ differential ring oscillator with process and temperature compensation was presented and implemented in typical $0.25\,\mu m$ CMOS technologies. Figure 4.17 shows the block diagram of the temperature and process compensated ring oscillator architecture proposed in [SAA06]. The bandgap reference generates stable reference voltage $V_{ref}$ from the available DC power supply $V_{dd}$. The voltage $V_{supply}$ generated from the stable $V_{ref}$ serves as the supply voltage for the temperature process compensation circuitry, replica feedback bias circuit, differential buffer delay ring oscillator and comparator. The temperature and process compensation circuitry generates the control voltage

$V_{ctrl}$ with respect to the current temperature and process conditions. The replica feedback bias circuit translates the control voltage $V_{ctrl}$ to the corresponding bias voltage $V_{Bp}$ and $V_{Bn}$ for the PMOS and NMOS parts in the differential buffer delay ring oscillator. The two output signals $V_{o1}$ and $V_{o2}$ of this ring oscillator with differential delay cells are usually inverted sine-wave signals, which should be inputted to the comparator in order to achieve the stable rectangular 2-phase non-overlapping clock signals $V_p$ and $V_n$ of required frequencies. Through the 4-phase clock generation circuitry composed of also process and temperature compensated circuits, the required 4-phase clock signals $V_{clka}$, $V_{clkb}$, $V_{clkc}$ and $V_{clkd}$ shown in Figure 4.6 can be obtained by changing the duty cycle and delay of the 2-phase non-overlapping clock signals $V_p$ and $V_n$. By modifying device parameters in this architecture suggested in [SAA06], a 20 $MHz$ process and temperature compensated 4-phase clock generator was designed and implemented in the high voltage ASIC "Balios".

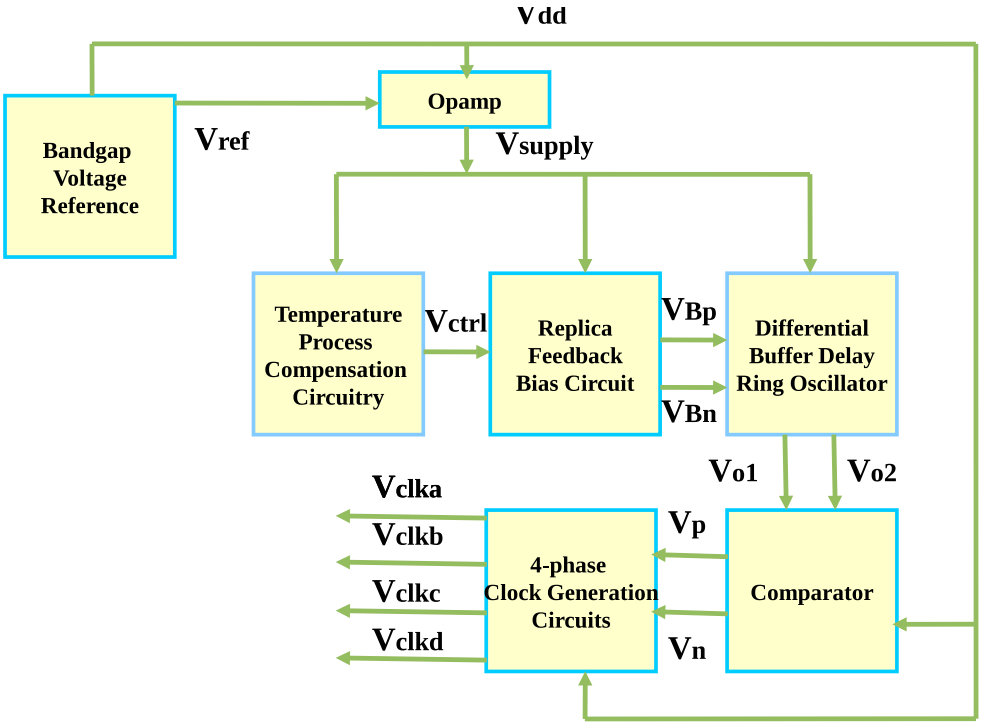



**Figure 4.17.:** Block diagram of the temperature and process compensated ring oscillator [SAA06].

In order to be able to apply external 2-phase or 4-phase clock signals as well, several demultiplexers controlled by enable signals $EN_1$ and $EN_2$ are included in the on-chip 4-phase clock generator for the 40-stage charge pump. Figure 4.19 shows the block diagram of the on-chip 4-phase clock generator. P and N stand for external 2-phase non-overlapping clock signals. A, B, C and D stand for external 4-phase clock signals. $O_1$ stands for the final output voltage of the high voltage charge pump "Balios". Figure 4.18 shows the post-layout simulation results of the designed on-chip 4-phase clock generator ($T = 47\,ns$, $T_1 = T_3 = 19.2\,ns$, $T_3 = T_4 = 4.3\,ns$).

The on-chip clock generation part in "Balios" is intended to increase the independency from external clock signals, so that a fully integrated high voltage generator can be implemented, which does not require any external clock signals.

### 4.3.2 Layout Implementation

The chip layout of "Balios" was designed similarly according to the high voltage layout design rules and techniques discussed in Section 3.3 and 4.2.1. The two implemented 4-phase clock generators

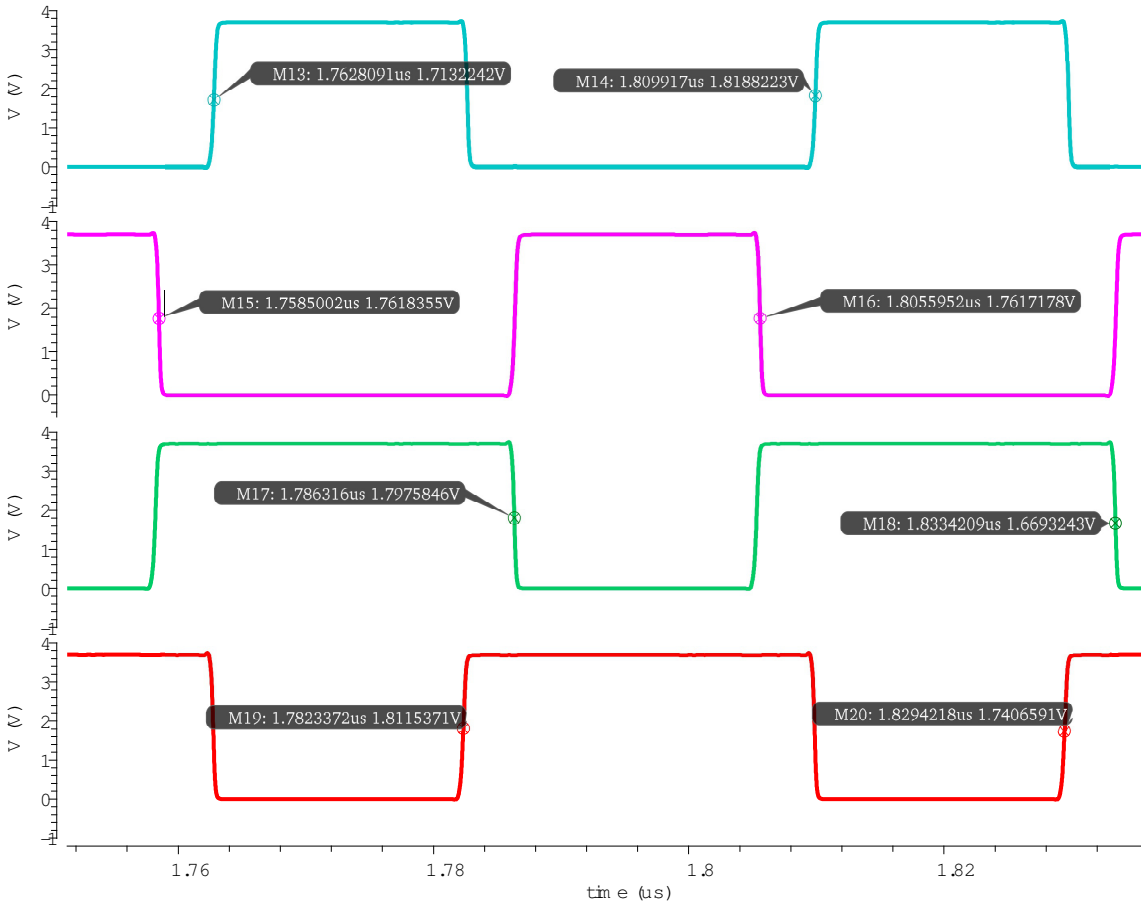



**Figure 4.18.:** Post-layout simulation result of the on-chip 4-phase clock generator inside "Balios" (signals from top to bottom: CLKa, CLKb, ClKc, ClKd).

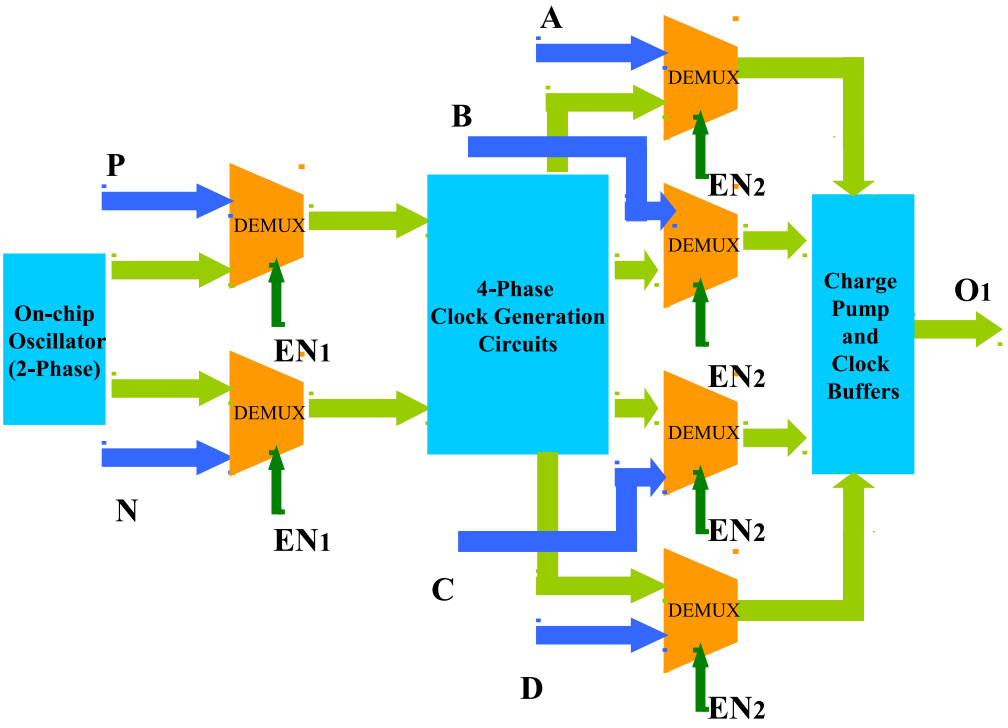



**Figure 4.19.:** Block diagram of the on-chip 4-phase clock generator inside "Balios".

are identical and follow the low voltage analog design rules and techniques. Good isolation between these low voltage blocks and the high voltage parts of the chip was considered during the layout design. For each 4-phase clock generator, the layout size is $0.68 \times 1.2 = 0.816\,mm^2$, which is displayed in Figure 4.20.

The whole chip layout of "Balios" including the 40-stage high voltage charge pump, 2 identical 4-phase clock generators, large clock drivers, several stabilizing capacitors between power and ground lines and all the necessary I/O pads can be found in Figure 4.21.

### 4.3.3 Measurement Results

The chip photograph of the second chip "Balios" packaged in JLCC84 is shown in Figure 4.22. In order to perform extensive investigation of this high voltage ASIC, an evaluation board shown in Figure 4.23 was designed and fabricated. It contains an on-board 2-phase clock generator to provide more reliable 2-phase clock signals. Connections for input output signals such as P, N, A, B, C and D in Figure 4.19 were implemented on this evaluation board.

After long time continuous operation, "Balios" shows good robustness and reliability at different operating temperatures. Due to the low overall power consumption of about $150\,mW$, where the 4-phase clock generator alone consumes about $15\,mW$, "Balios" has no self-heating problems. However, the average power efficiency at normal operations is round 10 %, which is lower than "Achilles" because of the additional clock generation parts. Figure 4.24 shows an example, when "Balios" was powered up without any external clock signals. At $V_{dd} = 3.7\,V$, $R_L = 1\,M\Omega$ and $C_L = 16\,pF$, "Balios" generates an output voltage approximately $120\,V$ within $300\,\mu s$. At the same operating conditions, the output voltage of "Balios" increases with the clock frequencies and DC supply voltages, respectively. Figure 4.25 shows the measurement results, when external 2-phase clock signals were applied, while Figure 4.26 shows the measurement results at $20\,MHz$ clock frequency and variable DC supply voltages. The measurement results demonstrate that if the charge pump circuit is designed at certain DC supply voltages and clock frequencies, its output voltage can be regulated by changing the applied DC supply voltages or clock frequencies. Nevertheless, it should be pointed out, that DC supply voltages and clock frequencies outside this range will probably cause the malfunction or damage of the charge pump circuit. For example, too high clock frequencies result in reduced output voltages of "Balios" due to insufficient charge transfer time for the designed pumping capacitors. Too high DC supply voltages above $5.5\,V$ will lead to the breakdown of the isolated low voltage transistors in "Balios".

### 4.3.4 Comparison and Discussion

The high voltage ASIC "Balios" is the second fully integrated charge pump using CMOS technologies after "Achilles", which is able to generate output voltages above $100\,V$ from low voltage DC power supplies with even smaller chip area due to the increased clock frequency.

The proposed 4-phase charge pump architecture in Figure 4.5 from Section 4.1.4 was once more proven to be effective and reliable for the on-chip high voltage generation. With more compact layout size of the charge pump part, there are more areas left in the ASIC, which can be used to implement other functionalities such as clock generation, digital processing, sensors etc. In "Bailos", the on-chip clock generation was already realized with sufficient isolation between high voltage and low voltage parts of the circuit. Therefore, "Balios" can be further considered as a high voltage SoC, which demonstrates the advantages to increase the integration level of on-chip high voltage generators.

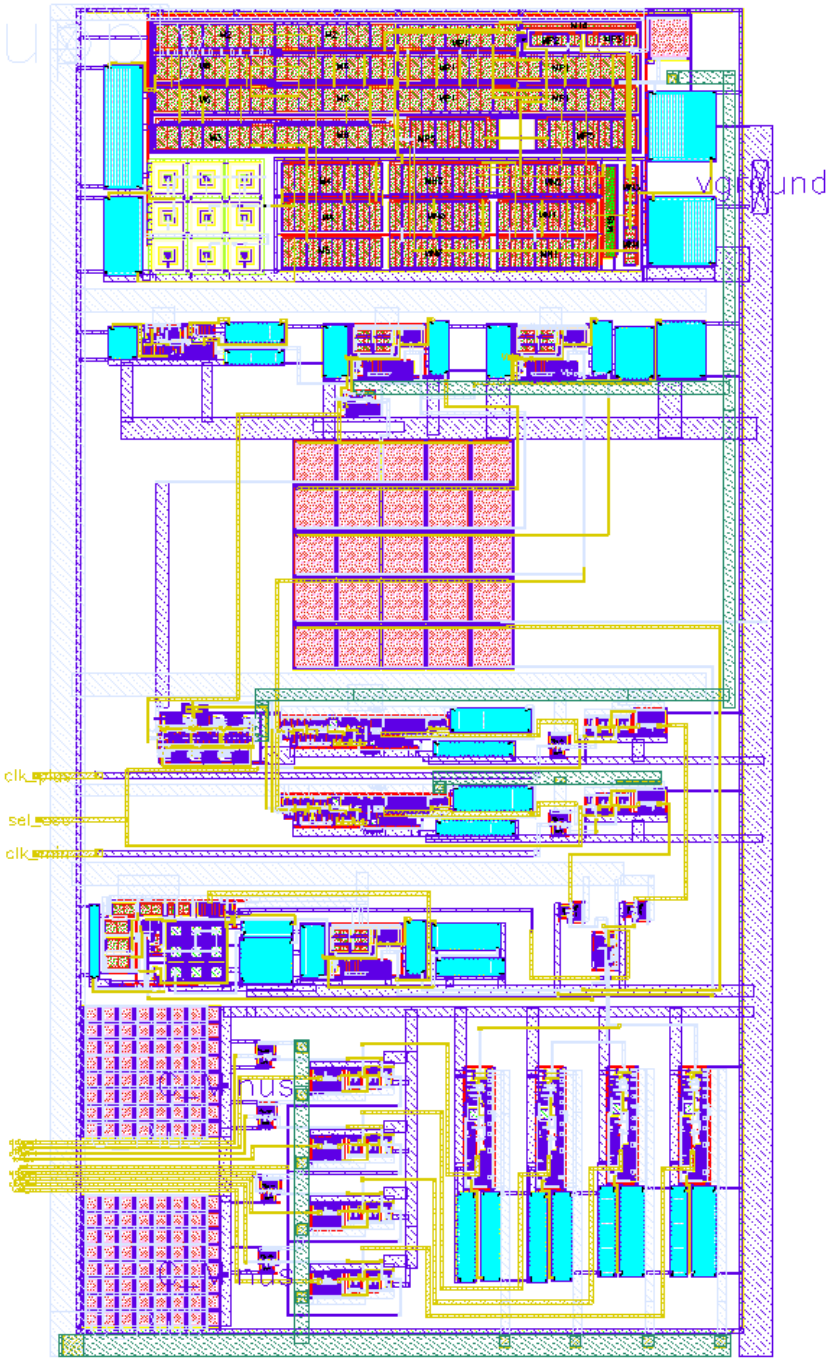


**Figure 4.20.:** Layout of the 4-phase clock generator inside "Balios".

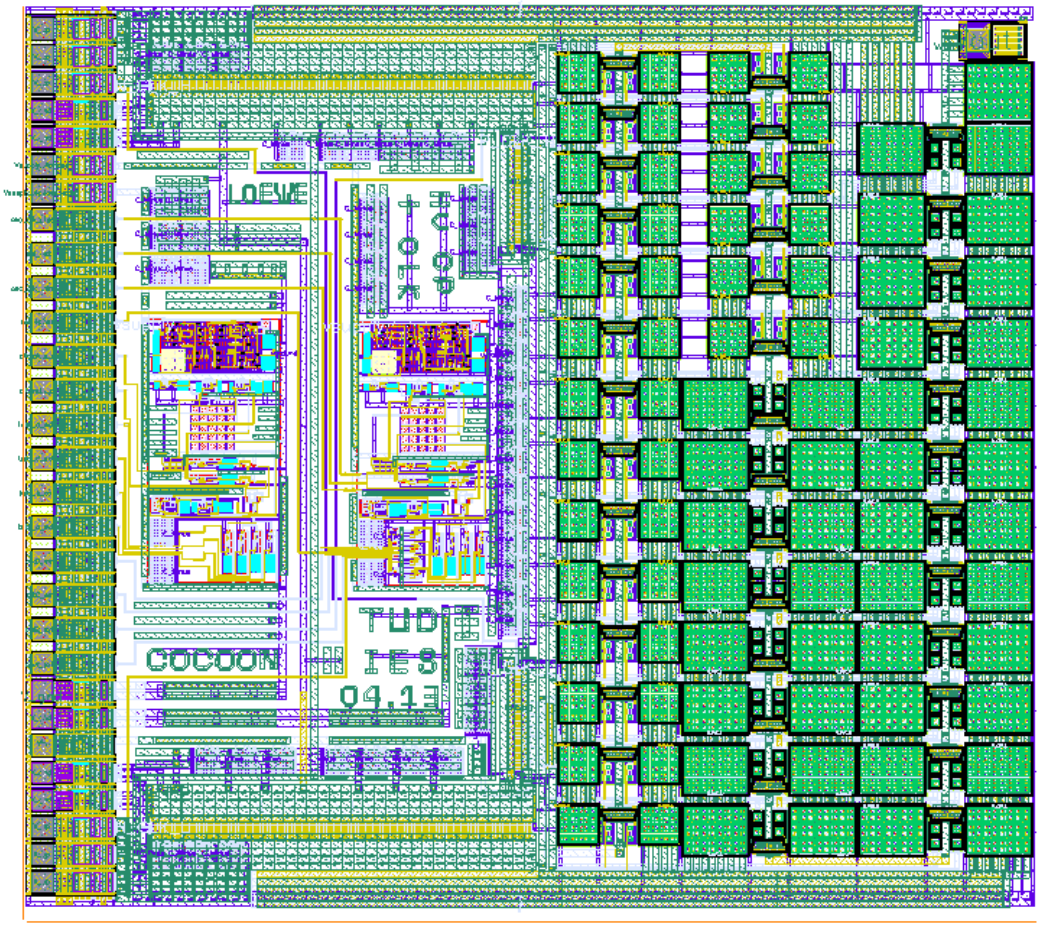



**Figure 4.21.:** Chip layout of the 40-stage proposed 4-phase charge pump "Balios" with on-chip clock generation.

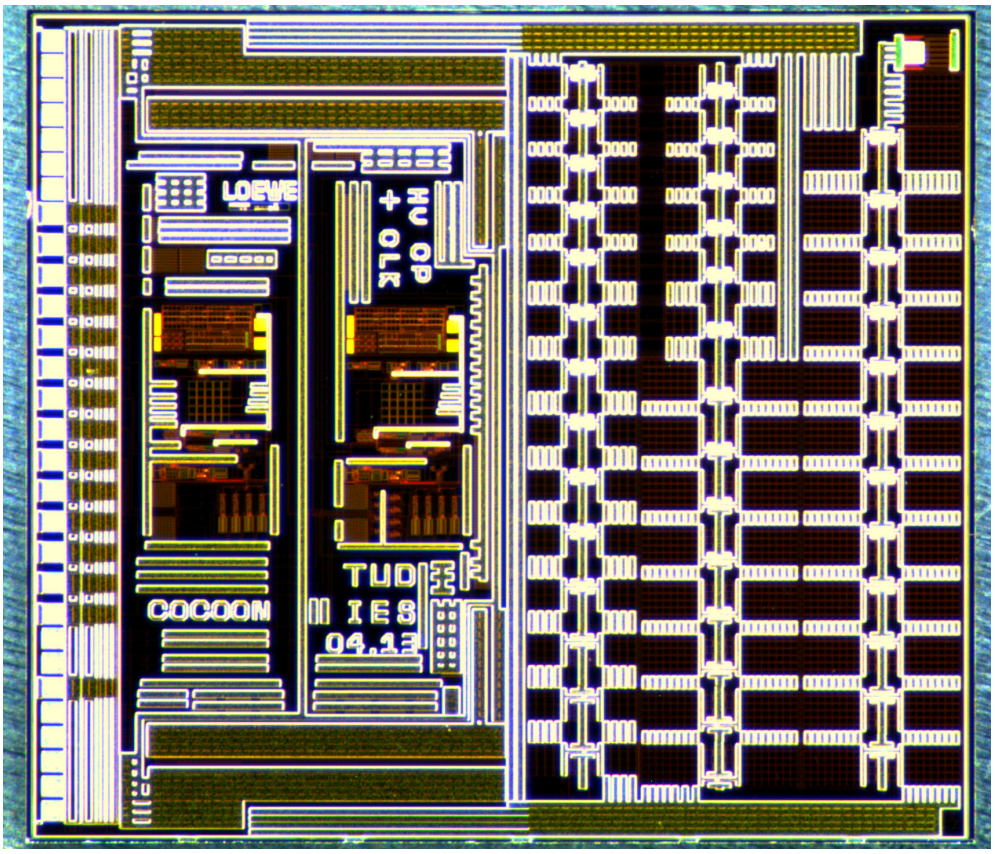



**Figure 4.22.:** Chip photograph of the 40-stage proposed 4-phase charge pump "Balios" with on-chip clock generation.

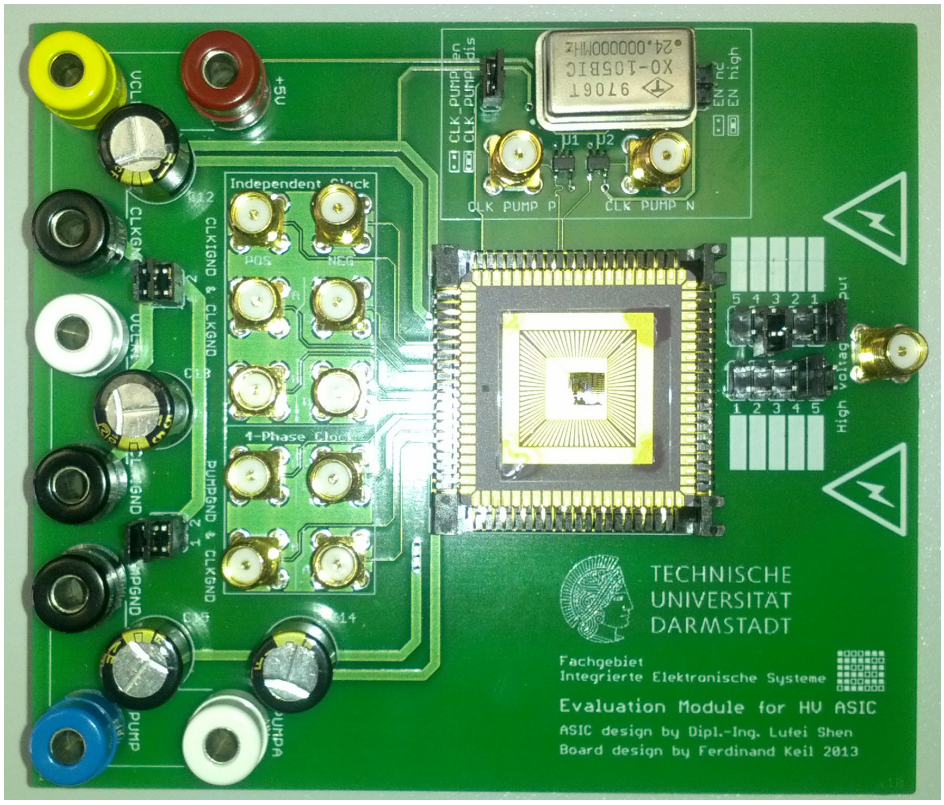



**Figure 4.23.:** Evaluation board of the 40-stage proposed 4-phase charge pump "Balios" with on-chip clock generation.

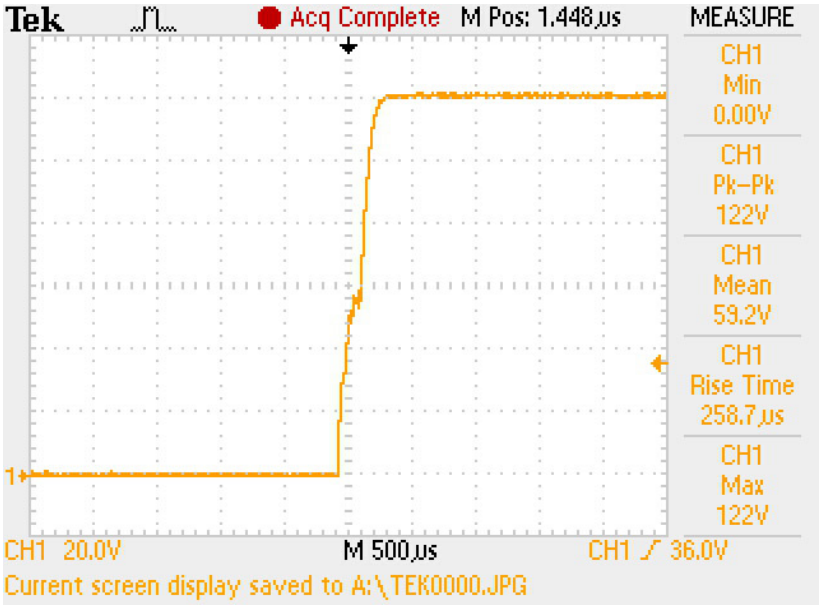



**Figure 4.24.:** Transient performance of the high voltage ASIC "Balios" without external clock signals.

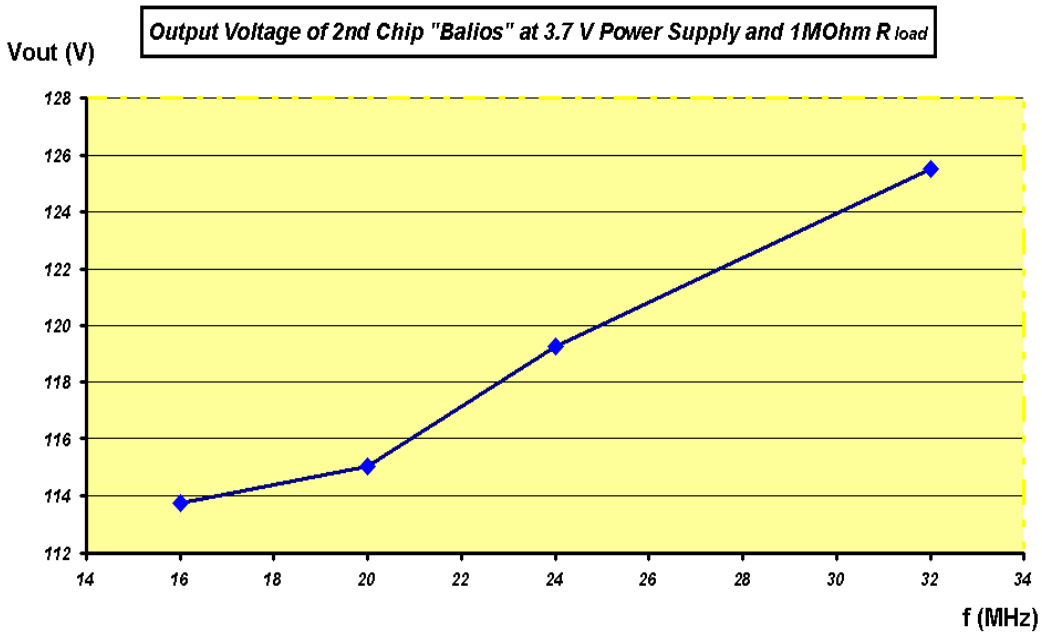



**Figure 4.25.:** Output voltages of the high voltage ASIC "Balios" at external clock signals of various frequencies.

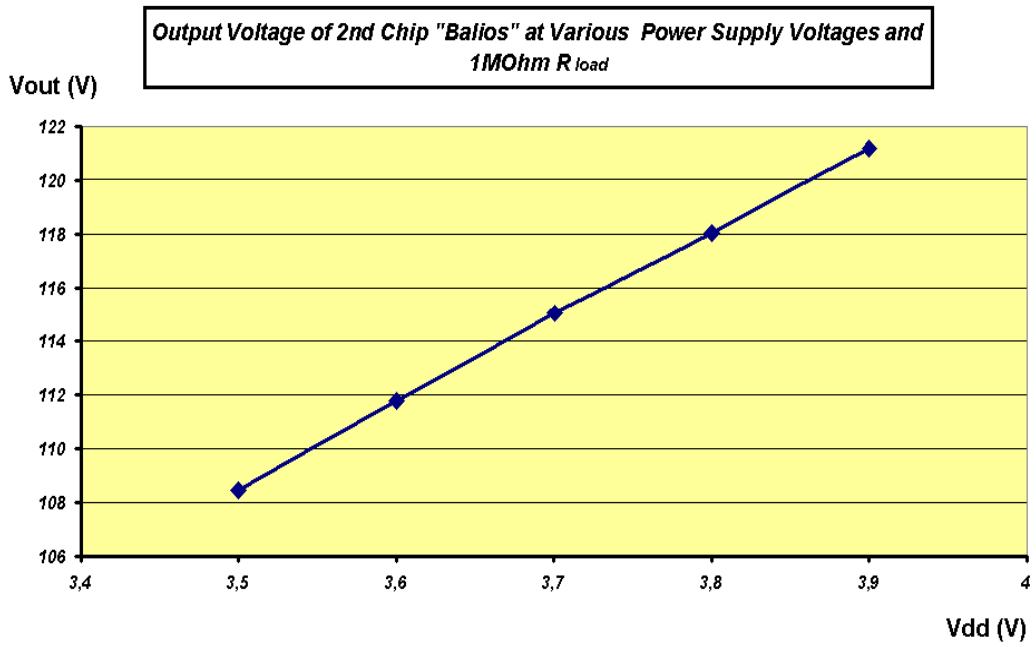



**Figure 4.26.:** Output voltages of the high voltage ASIC "Balios" with external 20 MHz clock signal at various DC supply voltages.

## 4.4 Advanced Clock Schemes with Dead Time Techniques for High Voltage Charge Pumps

The proposed 4-phase clock scheme with dead time techniques in Figure 4.6 shows significantly improved performance of charge pumps compared to the traditional 2-phase non-overlapping clock scheme. Hence, a comprehensive discussion about enhanced performance of integrated high voltage charge pumps by the introduction of other proposed advanced clock schemes with dead time techniques becomes of great importance. All the proposed 4-phase clock schemes with dead time techniques can introduce more efficient control signal strategies, so that the reverse current problem can be diminished. The theoretical analysis is supported by both simulation and experimental results, where the proposed 4-phase charge pump architecture in Figure 4.5 was adopted as the hardware platform.

### 4.4.1 2-phase Non-overlapping Clock Schemes

Charge pump circuits using the conventional 2-phase non-overlapping clock scheme suffer commonly from the reverse current problem: charge flows in the opposite direction back to the former stages due to the non-ideal switching of the charge transfer switches. Figure 4.27 illustrates an example of this clock scheme, which is applied in the charge pump circuit in Figure 4.5. $Clk_a$ and $Clk_c$ are the same clock signal. So are $Clk_b$ and $Clk_d$. It can be seen that at the non-ideal rising or falling edge of the clock waveforms, all the charge transfer switches at different stages will be shortly closed, which causes a certain amount of charge to flow back. With slower rising and falling time of the clock waveform, this reverse current problem becomes even more substantial. An example of the comparison between the conventional 2-phase non-overlapping clock scheme and the previously proposed 4-phase clock scheme regarding the reverse current is given in Figure 4.10.

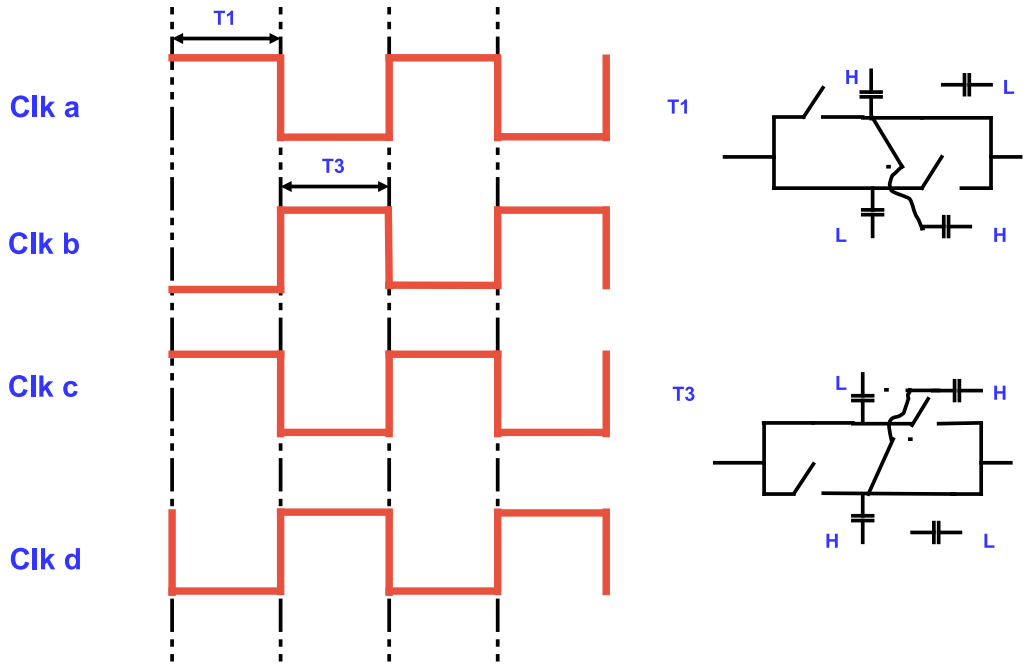



**Figure 4.27.:** Conventional 2-phase non-overlapping clock scheme.

### 4.4.2 2-phase Clock Schemes with Dead Time Techniques

2-phase clock schemes can also be employed together with dead time techniques to provide more control concepts of switches. However, it is usually not advantageous. Especially in circuits with both PMOS and NMOS switches, it can lead to undesired results. Figure 4.28 demonstrates an example of the failed application of dead time techniques in 2-phase clock schemes. Since clock signals during dead times are defined at one voltage level, both PMOS and NMOS switches can not be switched off at the same time. In the example in Figure 4.28, both PMOS switches are still switched on during the dead time $T_2$ and $T_4$, which leads to reverse currents in multistage charge pump circuits using the proposed 4-phase architecture. Furthermore, the output voltage swings with the clock voltage level due to the voltage drop over the large-sized pumping capacitors resulting in the charge flowing back from the load capacitor during the dead time $T_2$ and $T_4$. Additional switches or diodes must be added to the output of the circuit to stabilize the output voltage at the load capacitor, which result in considerable voltage drops of approximately $0.7\,V$ of the output voltage.

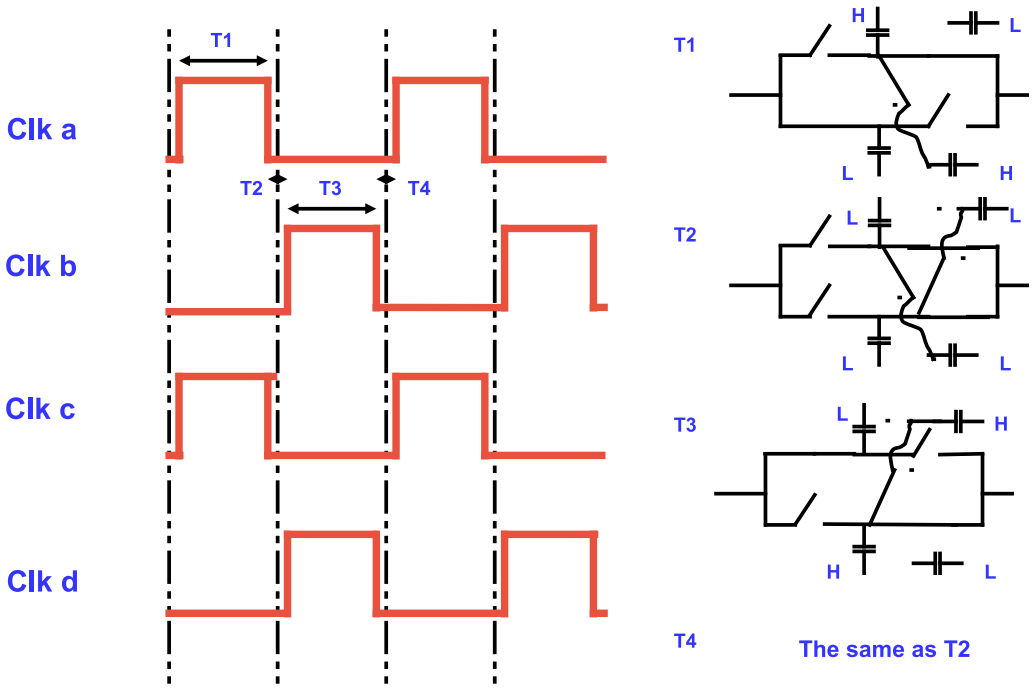



**Figure 4.28.:** 2-phase clock scheme with dead time techniques.

### 4.4.3 Proposed 4-phase Clock Schemes

In order to control each charge transfer switch separately and efficiently, 4-phase clock schemes are applied for such independency and precision of control signals for switches. Employing the proposed charge pump architecture in Figure 4.5, different 4-phase clock schemes can be discussed. The previously proposed 4-phase clock scheme in Figure 4.6 intends to avoid the short-time conduction of both NMOS and PMOS charge transfer switches at the clock switching time, by forcing all the switches to be switched off during the dead time $T_2$ and $T_4$.

The general idea to reduce reverse current is to disconnect the pumping capacitors with higher voltage levels at the current stage from those with lower voltage levels at the previous stage. In multistage circuits, the pumping capacitors at the current stage have lower voltage levels than those at previous stages, only when the pumping capacitors at the previous stage are connected to high

clock voltage levels and those at the current stage connected to ground or low clock voltage levels. Figure 4.7 in Section 4.1.4 shows three possible cases of reverse currents, which occur between cascaded stages at control signal switching time. The avoidance of these three possible types of reverse currents can be achieved by the introduction of dead time techniques.

Nevertheless, by using the proposed 4-phase clock scheme shown in Figure 4.6, some certain reverse currents still occur between cascaded stages at the moment when the charge transfer switches are switched on and off between the dead time $T_2$ or $T_4$ and the neighboring charge transfer phase $T_3$ or $T_1$, respectively. The cause for such reverse current is: The switch-on of the PMOS charge transfer switches and the switch-off of NMOS ones do not take place immediately due to the non-ideality of the control signals with non-negligible rising or falling time. There are always very short moments, when the PMOS charge transfer switches at the current charge pump stage and the NMOS ones at the next stage are both conducting. Obviously, at such switching time, the voltage levels of switch control signals are unstable. Hence, the cases of reverse currents shown in Figure 4.7 happen.

To further minimize such reverse currents in the previously proposed 4-phase clock scheme, a modified 4-phase clock scheme based on the modified channel width ratio between PMOS and NMOS transistors at the last stage of clock drivers is proposed in Figure 4.29.

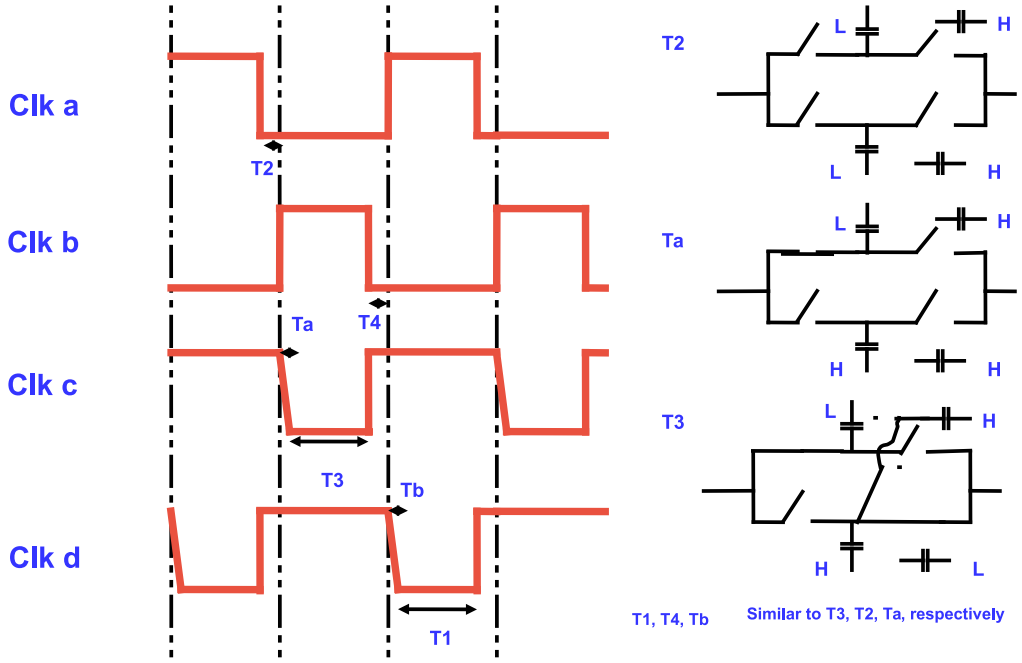



**Figure 4.29.:** Proposed 4-phase clock scheme with dead time techniques and modified channel width ratios of CMOS clock drivers.

In the clock scheme shown in Figure 4.29, one additional step is introduced between dead time $T_2$ or $T_4$ and charge transfer phase $T_3$ or $T_1$, respectively. These additional steps can be achieved by using clock drivers with high channel width ratios between PMOS and NMOS transistors at the last stage of the cascaded inverters, for example, a ratio of 10:1. Only the last stage of the clock drivers will affect the rising and falling edge of the output clock signals. It can be seen that the PMOS charge transfer switches at the current stage are closed only after the voltage levels of the pumping capacitors at the current stage are increased to the high voltage levels compared with the voltage levels of the pumping capacitors at the next stage. Hence, the 3 cases of reverse currents discussed in Figure 4.7 can be avoided. However, the drawback of this clock scheme is also self-evident. The charge transfer phase $T_1$ and $T_3$ are decreased by these additional steps, which should be carefully taken into account. The pumping capacitors should be able to be sufficiently charged

or discharged during $T_1$ or $T_3$. In reality, parasitic capacitors along the clock signal path can further decrease the slew rate of the clock signals, which can lead to even longer rising and falling times of clock signals than originally designed. As a consequence, undesired further reduction of the charge transfer duration $T_1$ or $T_3$ will occur in fabricated chips, although the post-layout simulations still show correct results.

Another advanced 4-phase clock scheme without changing parameters of devices to reduce reverse currents is proposed in Figure 4.30. In this clock scheme, the dead time $T_2$ and $T_4$ adopted in the previously proposed 4-phase clock scheme in Figure 4.6 are actually divided into two substeps, namely $T_{2a}$ and $T_{2b}$, or $T_{4a}$ and $T_{4b}$, respectively. The purpose of these two substeps is to disconnect all the cascaded neighboring stages from each other at the moment when the voltage level of the pumping capacitors begins to change. Principally, the three possible cases of reverse currents shown in Figure 4.7 will not happen.

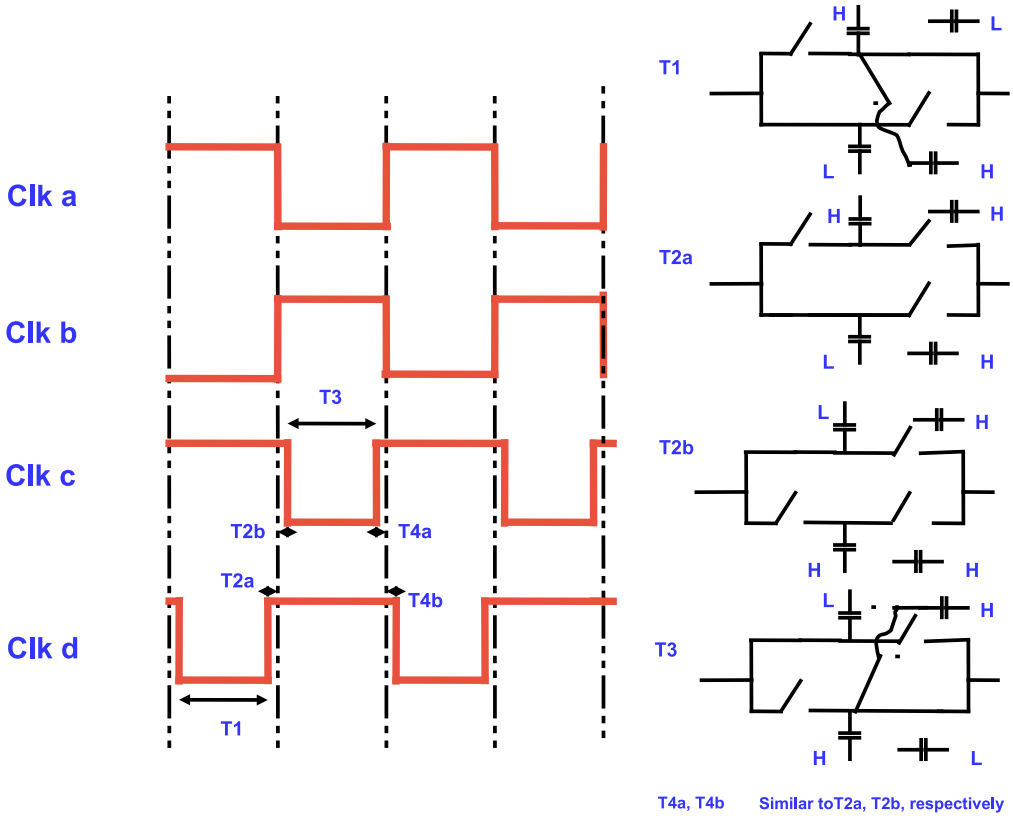



**Figure 4.30.:** Proposed 4-phase clock scheme with improved controlling of switches.

However, as analog switches, PMOS switches are more difficult to be completely switched off due to their required high gate control voltages. NMOS ones are much easier to be switched off, because they need only relatively low gate control voltages to be switched off and lower voltages can be more easily maintained. As a result, there are still certain reverse currents between the dead time substeps $T_{2a}$ and $T_{2b}$, or $T_{4a}$ and $T_{4b}$, when the PMOS charge transfer switches are short-timely switched on by the changing voltage level of the pumping capacitors at the cascaded next stage. The high voltage control signals of both PMOS charge transfer switches at the current stage are not high enough compared to this short-time high voltage spike at the input of the cascaded next stage, or at the output of the current stage, where one terminal of the PMOS switches is connected. Hence, another relatively small reverse current occurs. Furthermore, the generation and distribution of such a complex clock scheme can be difficult.

### 4.4.4 Comparison of Various Clock Schemes

To illustrate the characteristics of the 4-phase clock schemes proposed and discussed in Section 4.4.3, several simulations were performed under the Cadence (Virtuoso) environment. A 4-stage charge pump using the proposed 4-phase charge pump architecture shown in Figure 4.5 was employed as a comparison platform. The DC supply voltage and voltage level of the clock signals were set to $3.7\,V$. The load capacitor of the circuit was $1\,pF$, while there were no load resistors existing. The clock frequency was set to $10\,MHz$ with $5\,ns$ dead time ($T_2 = T_4 = 5\,ns$; $T_{2a} = T_{2b} = T_{4a} = T_{4b} = 2.5\,ns$). The comparison was between clock schemes presented in Figure 4.27, 4.6, 4.29, and 4.30. The clock scheme in Figure 4.28, namely the 2-phase clock scheme with dead time techniques was excluded for the comparison because of its known drawbacks of reverse currents discussed in Section 4.4.2. The simulation results are concluded in Table 4.8[5].

| **Clock Schemes** | $V_{out}(V)$ | **Power Consumption**($W$) |
|---|---|---|
| 2-phase non-overlapping | 17.61 | 2.234e-6 |
| Proposed 4-phase with dead time techniques | 18.25 | 2.268e-6 |
| Proposed 4-phase with modified channel width ratios of CMOS clock drivers | 18.35 | 2.049e-6 |
| Proposed 4-phase with improved controlling of switches | 18.26 | 0.848e-6 |

**Table 4.8.:** Comparison among different clock schemes.

In Table 4.8, the 2-phase non-overlapping clock scheme in Figure 4.27 shows the lowest output voltage with also very high power consumption. The proposed 4-phase clock scheme with dead time techniques in Figure 4.6 provides a good output voltage with correspondingly reasonable power consumption. The proposed 4-phase clock scheme with modified channel width ratios of CMOS clock drivers in Figure 4.29 achieves the highest output voltage with the second lowest power consumption. The proposed 4-phase clock scheme in Figure 4.30, which adopts more complex clock concepts but does not require any changes of device parameters, has the second highest output voltage and the lowest power consumption.

The simulation results in Table 4.8 can be further explained in details by the following figures illustrating the reverse currents between cascaded charge pump stages. As examples, the output current of the second stage at the 4-stage charge pump circuit is displayed, which has a positive current value for the reverse current.

Figure 4.31 shows that the reverse current is significant at the rising and falling edge of the 2-phase non-overlapping clock scheme, which is consistent with the theoretical analysis.

Figure 4.32 shows the reduced reverse currents at the moments between the dead time $T_2$ or $T_4$ and the neighboring charge transfer phase $T_3$ or $T_1$ in the proposed 4-phase clock scheme with dead time techniques in Figure 4.6, respectively. Although the peak values of these reverse currents are still significant, the amount of the charge flowing back is however much less than that in 2-phase non-overlapping clock scheme due to the shorter duration of these reverse currents.

Figure 4.33 demonstrates the output current waveform at the second stage of the 4-stage charge pump using the 4-phase clock scheme discussed in Figure 4.29. Thanks to the slower slew rate at the clock falling time of the clock signal $Clk_c$ and $Clk_d$, the reverse currents are almost negligible. For this reason, using this clock scheme, the highest stage voltage gain among all the discussed clock schemes can be achieved. However, the duration of charge and discharge of the pumping capacitors is decreased. And this clock scheme must be realized by the modification of device parameters such as width of transistors, which is sometimes not directly applicable.

[5] All capacitors are based on **Config.1** defined in Section 4.1.4.

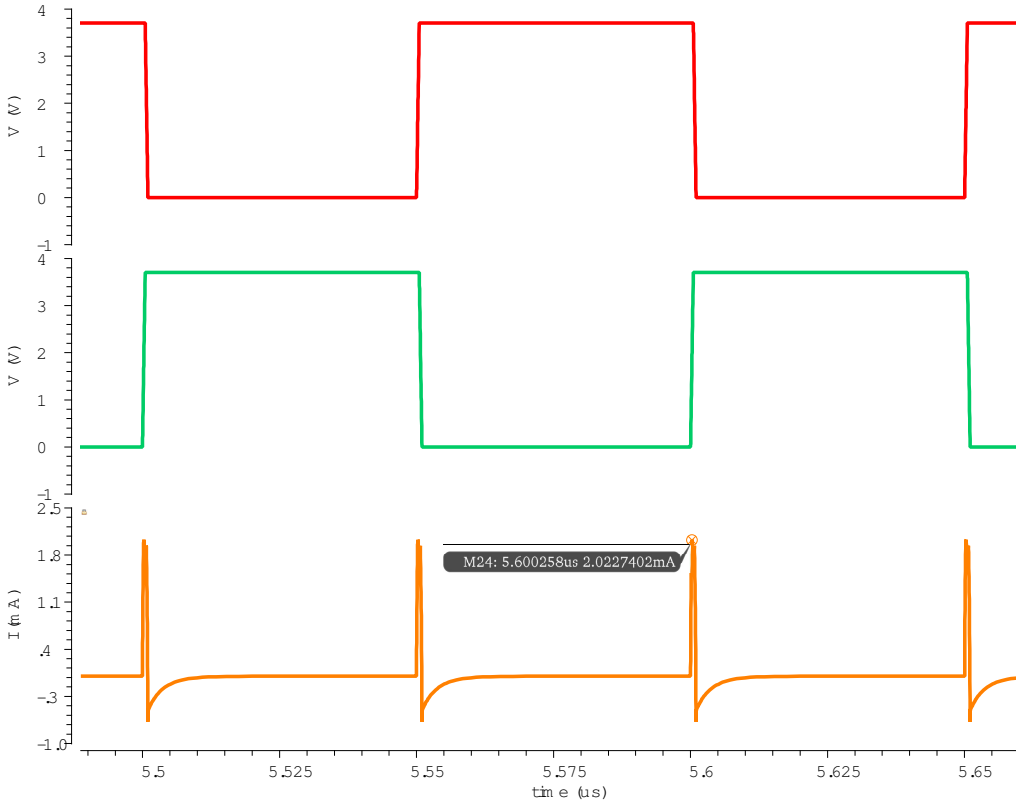



**Figure 4.31.:** Reverse currents in the 2-phase non-overlapping clock scheme (signals from top to bottom: CLKa, CLKb, Iout).

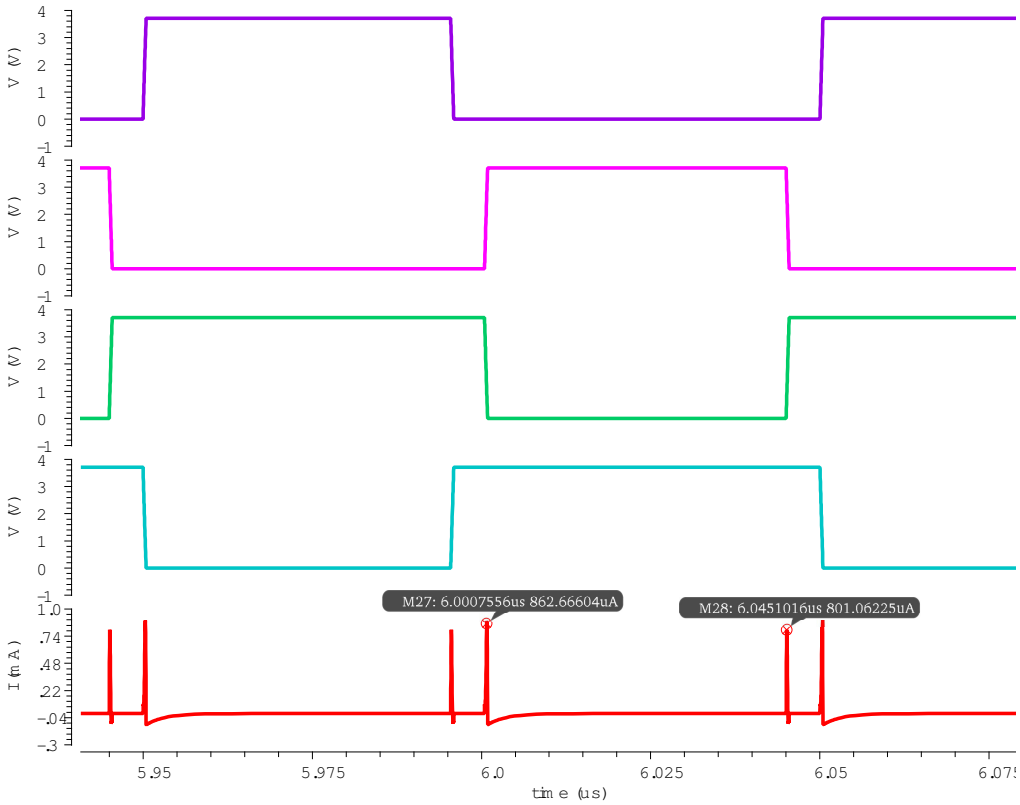



**Figure 4.32.:** Reverse currents in the proposed 4-phase clock scheme with dead time techniques (signals from top to bottom: CLKa, CLKb, ClKc, ClKd, Iout).

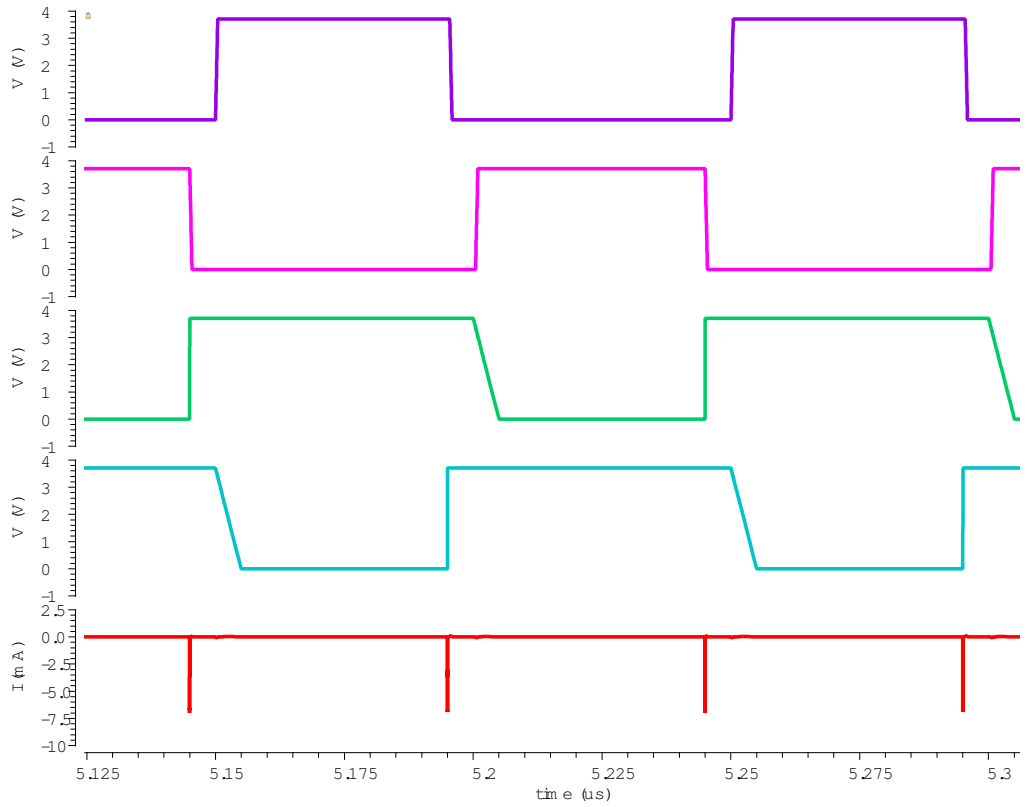



**Figure 4.33.:** Reverse currents in the proposed 4-phase with modified channel width ratios of CMOS clock drivers (signals from top to bottom: CLKa, CLKb, ClKc, ClKd, Iout).

Figure 4.34 demonstrates the reverse currents at the second stage of the charge pump circuit using the 4-phase clock scheme from Figure 4.30. It can be seen that at the switching time of $Clk_a$ and $Clk_b$ as the control signals of NMOS charge transfer switches, the Gate terminal voltage level of the PMOS charge transfer switches at the current charge pump stage becomes short-timely relatively low to keep switching off the PMOS switches due to the high voltage spike from the next stage. Therefore, a small amount of reverse currents with about 400 $\mu A$ current peak arises. Another negligible amount of reverse current with peak current approximately 140 $\mu A$ takes place, because at the switching time between $T_{2b}$ and $T_3$ , or $T_{4b}$ and $T_1$ , the large pumping capacitors are beginning to charge the small control capacitors at the same stage, which reduces the voltage levels of the pumping capacitors short-timely. Therefore, there is a temporary negative voltage difference between the connected pumping capacitors at the current and next stage.

### 4.4.5 Experimental Results

Several measurements were accomplished by means of the fabricated fully integrated 36-stage charge pump circuit "Achilles" shown in Figure 4.16 from Section 4.2. Virtex-6 FPGA ML605 evaluation board was adopted as the 4-phase clock generator to generate a clock period of 102 $ns$ with 6 $ns$ dead time. External clock drivers were used to increase the clock voltage level to 3.7 $V$ or 3.3 $V$ from the 2.5 $V$ output voltage level of the evaluation board. The clock schemes from Figure 4.27, 4.6 and 4.30 were implemented. The clock scheme with modified channel ratios of transistors at clock drivers in Figure 4.29 could not be implemented due to the on-chip clock drivers inside the test chip. Because only the last stage of the on-chip clock drivers in "Achilles" can influence the rising and falling time of the final clock signals applied to the 36-stage charge pump, any modification of the

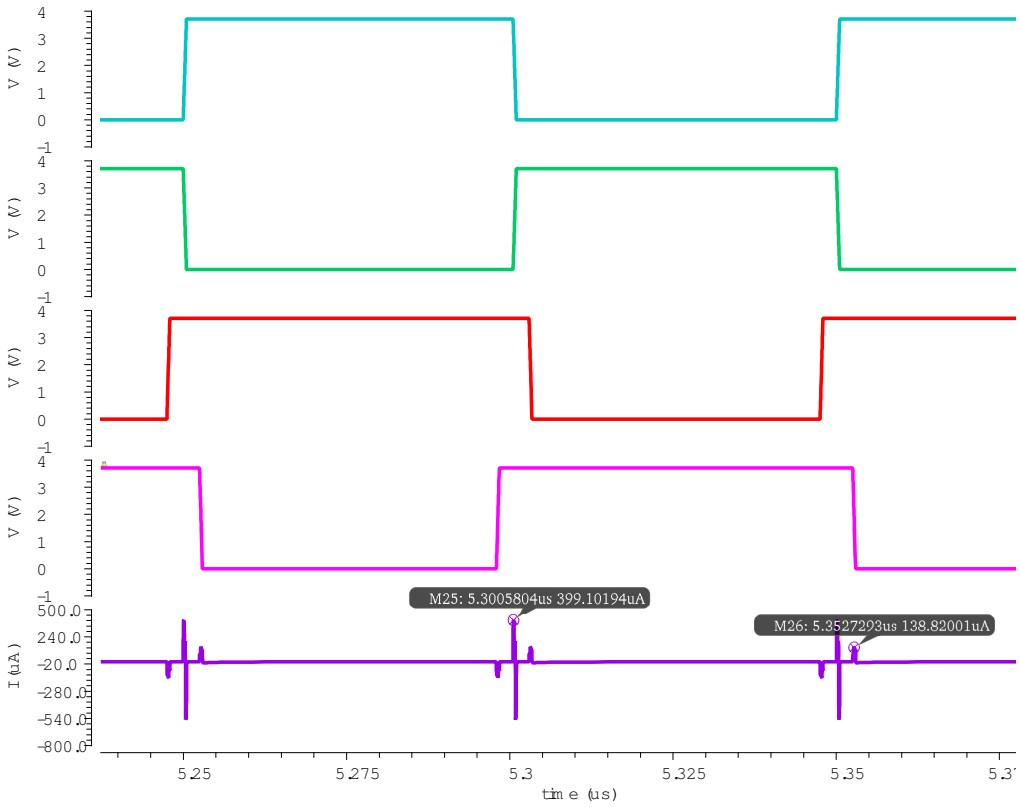



**Figure 4.34.:** Reverse currents in the proposed 4-phase with improved controlling of switches (signals from top to bottom: CLKa, CLKb, ClKc, ClKd, Iout).

external clock drivers will not be useful. For all the measurements, the equivalent load resistor $R_L$ at the test chip was 910 $k\Omega$, and the equivalent load capacitor $C_L$ was 61 $pF$.

Table 4.9 shows the measurement results for different clock schemes at 3.3 $V$ DC power supply, when no load resistor exists. With no load resistors, "Achilles" will generate higher than 120 $V$ output voltage at 3.7 $V$ DC power supply, which exceeds the related maximum allowed operating voltage of the 120 $V$ CMOS technology H35. Table 4.10 displays the measurement results with the load resistor of 910 $k\Omega$. $V_{dd}$ and $I_{dd}$ in both tables are the voltage and current from the DC power supply.

| **Clock Schemes** | $V_{out}(V)$ | $I_{dd}(mA)$ | $V_{dd}(V)$ |
|---|---|---|---|
| 2-phase non-overlapping | 104 | 20.055 | 3.3 |
| Proposed 4-phase with dead time techniques | 116 | 19.244 | 3.3 |
| Proposed 4-phase with improved controlling of switches | 118 | 19.130 | 3.3 |

**Table 4.9.:** Measurement results of different clock schemes without load resistors.

The negative influence of an extensively long duration of dead time, which reduces the charge transfer duration is shown in Table 4.11 based on the proposed 4-phase clock scheme in Figure 4.6 ($R_L = 910\,k\Omega$, $C_L = 61\,pF$, $V_{dd} = 3.7\,V$). It can be concluded that a suitably short dead time duration should be taken into account during the introduction of dead time techniques.

The measurement results correspond closely to the theoretical analysis and simulation results, which support the advantages of the proposed 4-phase clock schemes.

| Clock Schemes | $V_{out}(V)$ | $I_{dd}(mA)$ | $V_{dd}(V)$ | Efficiency($\eta$) |
|---|---|---|---|---|
| 2-phase non-overlapping | 96.7 | 25.97 | 3.7 | 10.69 % |
| Proposed 4-phase with dead time techniques | 111 | 25.30 | 3.7 | 14.46 % |
| Proposed 4-phase with improved controlling of switches | 111 | 24.97 | 3.7 | 14.65 % |

**Table 4.10.:** Measurement results of different clock schemes with the load resistor of 910 kOhm.

| $V_{out}(V)$ | $I_{dd}(mA)$ | Duration of Dead Time($ns$) |
|---|---|---|
| 111 | 25.30 | 6 |
| 111 | 25.76 | 9 |
| 111 | 25.80 | 12 |
| 110 | 26.02 | 15 |
| 108 | 26.16 | 21 |

**Table 4.11.:** Measurement results of different dead time durations.

### 4.4.6 Discussion

In principle, the dead time duration should be as short as possible, but it is usually difficult to generate very short dead time durations such as 1 $ns$ due to the non-ideal rising and falling time of clock signals. Besides, dead times are mostly generated through delay cells, which are sensitive to the PVT variations of the clock generation circuits. Some PVT compensation methods are helpful to improve the accuracy of the dead time generation [SAA06].

The proposed 4-phase clock schemes with dead time techniques are proven to be able to support higher stage voltage gain by reducing reverse currents between cascaded charge pump stages compared with the traditional 2-phase non-overlapping clock scheme. Especially the 4-phase clock scheme proposed in Figure 4.6 is more suitable in practice due to its simplicity compared with other proposed 4-phase clock schemes.

## 4.5 Stabilization Methods for Integrated High Voltage Charge Pumps

From the measurement results of the high voltage ASIC "Balios" introduced in Section 4.3, it can be concluded that stabilization methods are essential in charge pump circuits. Due to unstable clock signals, imprecise pumping capacitor values, different operating temperatures etc., which are basically all caused by PVT variations, the designed output voltage can usually not be exactly achieved at given operating conditions. Furthermore, with unstable load resistors, it is also difficult to reach required output voltage levels. Stabilization methods are not only for improved voltage performance but also for robustness and reliability of integrated high voltage charge pumps. If the generated final output voltage of charge pumps exceeds the maximum allowed operating voltage of the chosen CMOS technology, or dramatic voltage (current) changes occur at certain devices in charge pumps, the reliability of the entire chip will be considerably affected. In this section, different stabilization methods which are intended to be applied in fully integrated high voltage charge pumps are discussed and proven by measurement results based on the high voltage ASIC "Balios".

### 4.5.1 Feedback Regulation by Adjusting DC Power Supply or Clock Frequency

Since the voltage performance of the charge pump circuit will be influenced by many factors such as changes of load currents, noises at the DC voltage supply, mismatching of integrated capacitors, unbalanced delays in the clock distribution etc., the feedback regulation is necessary to stabilize the output voltage of charge pumps.

The output voltage of charge pumps is usually a function of the DC power supply $V_{dd}$, pumping capacitor value $C$, clock frequency $f$, load current $I_L$ and stage number $n$. Equation 4.4 in Section 4.1.2 shows the relationship between the output voltage of Pelliconi charge pump and those parameters mentioned above [PR03]. The two fully integrated charge pump chips "Achilles" in Section 4.2 and "Balios" in Section 4.3 are based on Pelliconi charge pump. Once the circuit is designed, the only easily changeable parameters are the DC power supply $V_{dd}$, clock frequency $f$, and load current $I_L$. Changing the pumping capacitor value $C$ or stage number $n$ needs complicated hardware reconfigurations, which are usually difficult to realize. The load current $I_L$ can be principally controlled by high voltage linear regulators at the output of charge pumps. However, linear regulators have low power efficiency and consume alone large static currents, which significantly reduce the output voltage of charge pumps and are not suitable for low power integrated high voltage charge pumps. Therefore, the feedback regulation regarding the DC power supply $V_{dd}$ and clock frequency $f$ is mainly discussed.

Figure 4.35 explains the principle of the feedback regulation by adjusting the DC power supply. The low voltage boost buck (step-up and step-down) charge pump circuit provides suitable DC power supply voltages between e.g. $3\,V$ and $5\,V$ from the available low battery voltage such as $3.7\,V$. This step-up or step-down voltage generation depends on the control voltage $V_{ctrl}$, which is generated from the feedback voltage $V_{fb}$ and the reference voltage $V_{ref}$ with the aid of the error amplifier. Once the feedback voltage $V_{fb}$ is determined by the fixed voltage divider for the required output voltage $V_{out}$, this concept can realize the stabilization of the output voltage $V_{out}$ of the charge pump circuit.

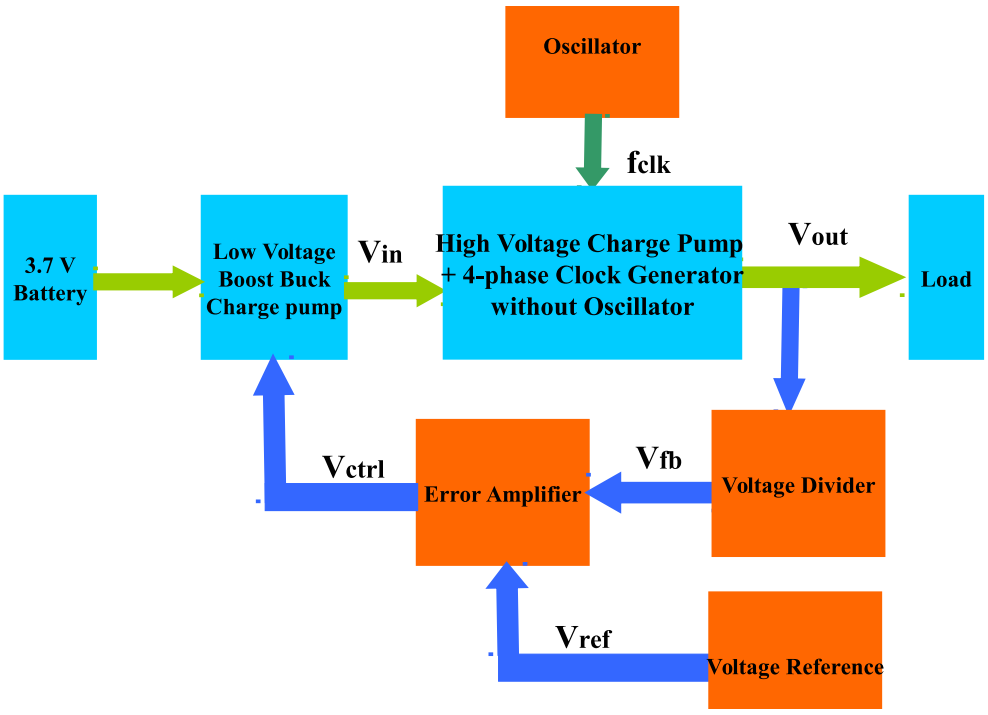



**Figure 4.35.:** Feedback regulation by adjusting DC power supply.

Figure 4.36 presents the principle of the feedback regulation by adjusting the clock frequency $f$ of the charge pump circuit. The low voltage charge pump is supposed to provide the stable DC supply voltage $V_{dd}$ for the high voltage charge pump. It can be omitted, if the battery voltage remains stable during the whole operation. The voltage controlled oscillator speeds up or slows down the clock frequency $f$ according to the control voltage $V_{vco}$, which is generated by the error amplifier depending on the comparison between the reference voltage $V_{ref}$ and feedback voltage $V_{fb}$. The feedback voltage $V_{fb}$ is defined by the required output voltage $V_{out}$ through the fixed voltage divider. At higher or lower output voltage levels than the required one, the clock frequency $f$ provided by the voltage controlled oscillator will correspondingly decrease or increase. Hence, the stabilization of the output voltage $V_{out}$ of the charge pump can be achieved.

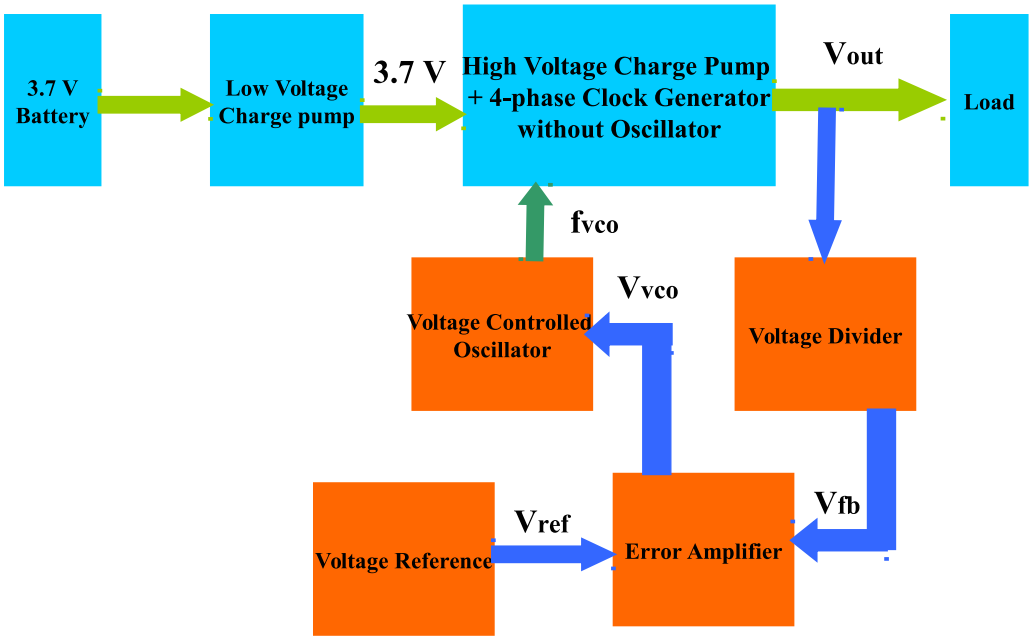



**Figure 4.36.:** Feedback regulation by adjusting clock frequency.

In both feedback regulation methods, the influences of clock schemes on the output voltage are not related. As discussed in Section 4.1.4, the operation of the charge pump circuit directly under 2-phase clock signals shows lower output voltage and power efficiency compared with the proposed 4-phase clock scheme mainly due to the reverse current problem. However, the adopted clock scheme is usually not directly related to the feedback regulation concepts.

### 4.5.2 Other Stabilization Methods

Due to the maximum allowed operating conditions of certain devices, especially of isolated low voltage transistors in the integrated charge pump circuit, and the maximum operating voltage of chosen high voltage CMOS technologies, some other stabilization methods are essential to ensure the robust and reliable operation of the circuit and to protect the circuit from permanent damages. The proposed 4-phase charge pump architecture in Figure 4.5 employs isolated (triple-well) low voltage transistors, whose horizontal breakdown voltage between Drain and Source (Gate) terminals is still low voltage e.g. maximum 5.5 $V$. Their vertical breakdown voltage from each terminal of the transistors to the p-substrate reaches the high reverse breakdown voltage between the underlying deep NWELL and p-substrate. For this reason, the DC power supply should be kept lower than

5.5 $V$ to avoid the Drain-Source breakdown voltage of those isolated low voltage transistors. Any drastic change of load currents, which induces the short-time voltage difference higher than 5.5 $V$ between the output voltage and the voltage levels at pumping capacitors of the last stage, should be avoided. Besides, high voltage CMOS technologies can not withstand voltage levels higher than their maximum operating voltages. The output voltage of the charge pump should not exceed the given operating voltage limits.

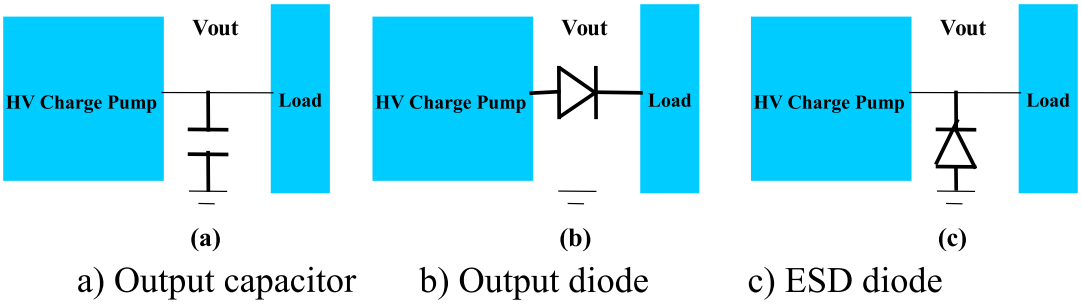



**Figure 4.37.:** Other stabilization methods.

Figure 4.37 demonstrates three possible stabilization methods for the robustness and reliability of charge pump circuits, assuming that the DC power supply voltage is kept within the tolerable range for all the devices.

- **Case a:** The high-capacitance load capacitor can not only smooth the output voltage by reducing the voltage ripple, but also decrease abrupt output voltage drops. Because of the adequate charge amount stored at this large load capacitor, abrupt changes of load currents can be compensated, so that only small voltage difference under the safe limit for isolated low voltage devices will be caused. The long charge or discharge time also provides the charge pump circuit enough time to reach the new stable condition at higher or lower voltage levels. However, this method can only handle slight changes of load currents, since integrated capacitors have usually low capacitor values of several picofarad. In extreme cases such as abrupt short-circuit at the load, the output voltage (current) difference will be too large, which leads to the damage of devices. In addition, large load capacitors increase the ramp-up time and recovery time of the charge pump circuit, which is not preferred in high speed applications.

- **Case b:** Output diodes with high reverse breakdown voltages are used to protect the charge pump circuit from the high voltage spike at the load. Nevertheless, in step-up high voltage charge pumps (high voltage generators), the output voltage is the highest voltage level in the circuit. If the load current decreases, the output voltage of the charge pump will reach a higher voltage level safely (similar to the start-up of the charge pump) in the case that the final output voltage is still lower than the maximum operating voltage of the chosen technology. If the load current increases, the output voltage of the charge pump with such output diodes will reach a lower voltage level. Those output diodes will be then in the forward conduction, which provides no protection against sudden output voltage drops. Therefore, such stabilization method with only output diodes with about 0.7 $V$ additional and undesired voltage drop of the output voltage, is merely useful, when inductive load or high voltage spikes exist, which can lead to the breakdown of the isolated low voltage transistors in the charge pump.

- **Case c:** ESD diodes such as Zener diodes are applied to prevent the output voltage of charge pumps from exceeding the maximum operating voltage of chosen technologies. They can be easily integrated into the circuit and limit the output voltage below their reverse breakdown voltage levels. However, in such cases, currents through these ESD diodes should be controlled

under the current limitation of those diodes, which are in principle wasted. Hence, this stabilization method is normally only for the protection of charge pump circuits against output voltages exceeding the technology limits.

### 4.5.3 Experimental Results

Two test circuits based on the second chip "Balios" were built to verify the output voltage stabilization methods by adjusting the DC power supply and clock frequency, respectively. The following ICs (Integrated Circuit) were adopted to realize the function blocks shown in Figure 4.35 and 4.36: voltage controlled oscillator: 74HC4046 [VD14]; low voltage boost buck charge pump: MCP1253-ADJ [MAI14]; voltage reference: REF192GPZ [Dat14e]; error amplifier: AD823ANZ [Dat14a]. To investigate the thermal behavior of the test circuits, the conditioning cabinet HC4005 was applied to vary the operating temperatures from 20 °C to 100 °C. The measurement environment is illustrated in Figure 4.38.

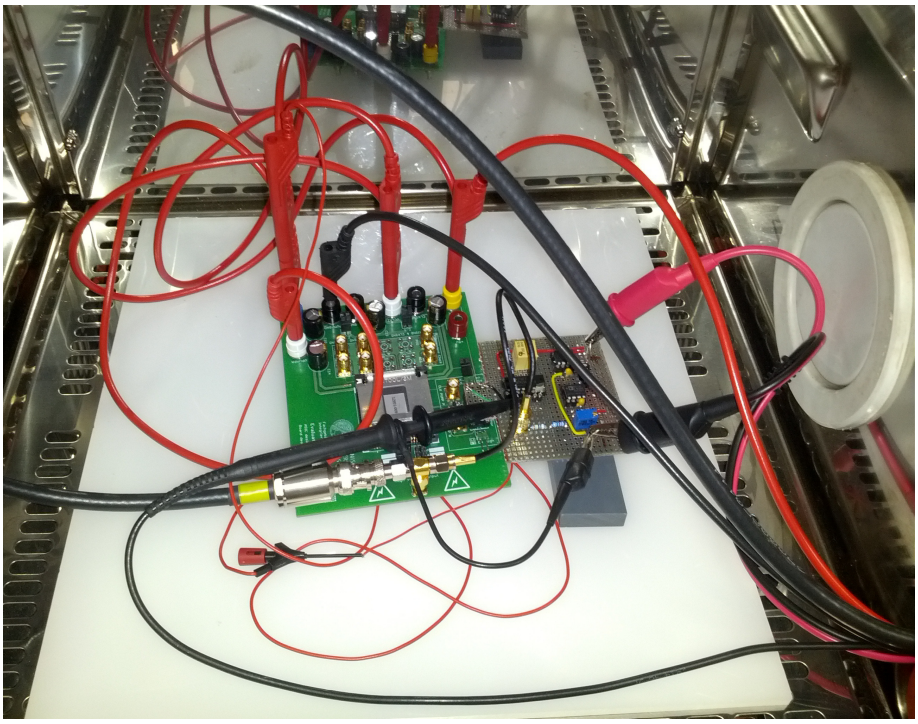


**Figure 4.38.:** Test circuits in the conditioning cabinet HC4005.

In Figure 4.39, the measurement results of the feedback regulation method by adjusting the clock frequency at the room temperature are displayed. The effective feedback regulation of the output voltage of the charge pump circuit operates properly, so that the output voltage remains at the previously selected value $110\,V$. The clock frequency of the voltage controlled oscillator is regulated by the feedback voltage $V_{fb}$ between 10 and $26\,MHz$. In Table 4.12, the measurement results prove the stability of this clock frequency feedback regulation against the variations of the environmental temperature. The increase of the clock frequency at higher temperatures can be explained by the non-linearity of the discrete components and ICs, while the output voltage of the charge pump is still stabilized[6].

[6] All these measurements were based on $V_{dd} = 3.686\,V$, $C_L = 106\,pF$.

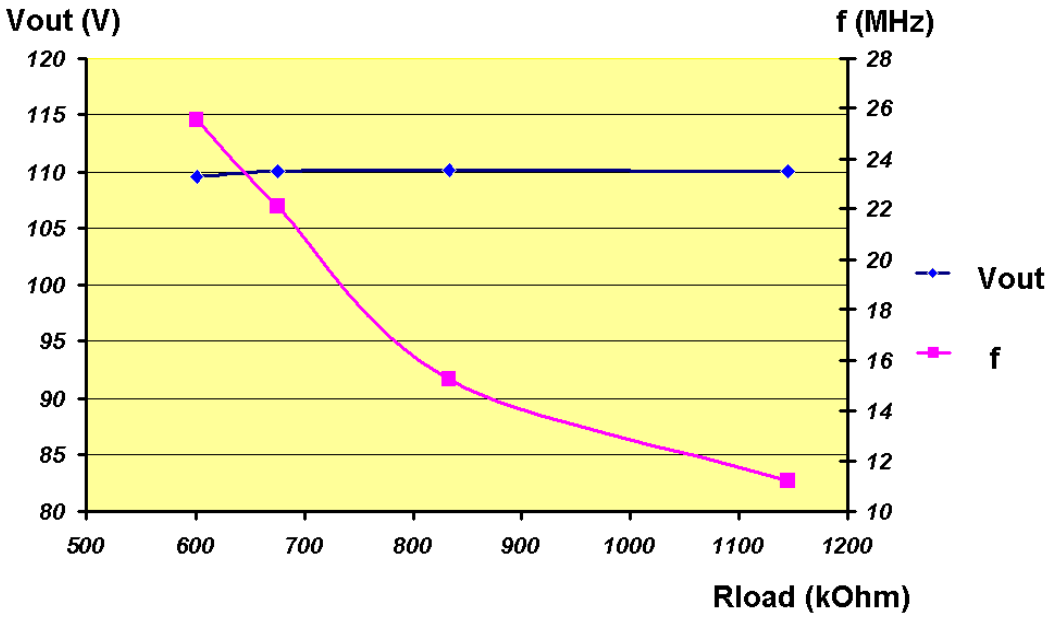



**Figure 4.39.:** Measurement results of the feedback regulation by adjusting the clock frequency.

| **Temperature**(°C) | $V_{out}(V)$ | $f_{vco}(MHz)$ | $R_L(k\Omega)$ |
|---|---|---|---|
| 20 | 110.11 | 15.249 | 833 |
| 40 | 110.21 | 15.373 | 833 |
| 60 | 110.47 | 15.586 | 833 |
| 80 | 110.87 | 16.033 | 833 |
| 100 | 111.05 | 18.64 | 833 |

**Table 4.12.:** Measurement results of the feedback regulation by adjusting the clock frequency at different temperatures.

In Figure 4.40, the measurement results of the feedback regulation method by adjusting the DC power supply at the room temperature are also displayed. By regulating the DC supply voltage for the charge pump through the feedback circuits, the output voltage of the charge pump is stabilized at the previously selected value $110\,V$ at various load resistors. In Table 4.13, good stability of the voltage performance against the variations of the environmental temperature is demonstrated in spite of the non-linearity of the discrete components and ICs[7].

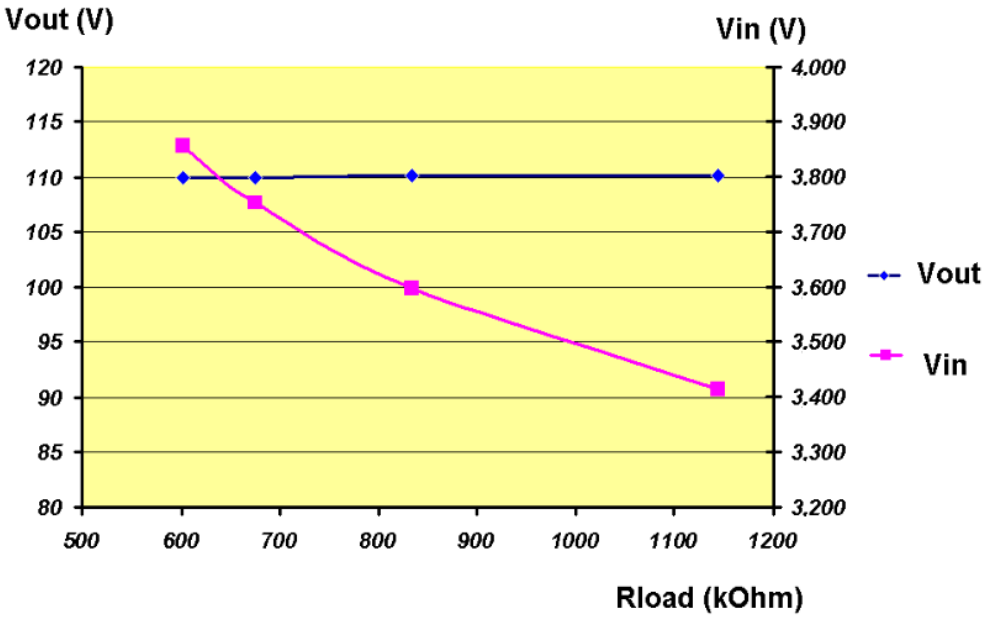



**Figure 4.40.:** Measurement results of the feedback regulation by adjusting the DC power supply.

| **Temperature**(°C) | $V_{out}(V)$ | $V_{dd}(V)$ | $R_L(k\Omega)$ |
|---|---|---|---|
| 20 | 110.1 | 3.598 | 833 |
| 40 | 110.1 | 3.598 | 833 |
| 60 | 110.1 | 3.602 | 833 |
| 80 | 109.9 | 3.603 | 833 |
| 100 | 110.2 | 3.626 | 833 |

**Table 4.13.:** Measurement results of the feedback regulation by adjusting the DC power supply at different temperatures.

The stabilization method using load capacitors for the robustness and reliability of the circuit was investigated experimentally. Table 4.14 shows the measurement results at different load capacitors, when the charge pump circuit was without any feedback regulation and the load resistor was changed from $910\,k\Omega$ to $476\,k\Omega$ abruptly at room temperature[8]. The value of the load capacitor does not affect the stable value of the output voltage $V_{out}$. However, it does influence the instant output voltage drop $V_{ripple}$ and the recovery time for the charge pump to reach the new stable state. Larger load capacitors reduce the short-time output voltage drop, increases the robustness and reliability of the circuit, but cause also a very long recovery time. The abrupt increase of the load resistors has

[7] All these measurements were based on $f_{vco} = 20\,MHz$, $C_L = 106\,pF$.
[8] All these measurements were based on $f_{vco} = 20\,MHz$, $V_{dd} = 3.7\,V$.

similar effects. It will mostly not damage charge pump circuits, when the output voltage of charge pumps is limited by Zener diodes under the maximum operating conditions of the chosen technology.

| $C_L$ | $V_{out}(V)$ | $\Delta V_{out}$ **in the first 100** $\mu s$ $(V)$ | **Recovery Time** | $R_L(k\Omega)$ |
|---|---|---|---|---|
| 6 $pF$ | 114 → 100 | 14 | 50 $\mu s$ | 910 → 476 |
| 16 $pF$ | 114 → 100 | 14 | 100 $\mu s$ | 910 → 476 |
| 100 $pF$ | 114 → 100 | 12 | 150 $\mu s$ | 910 → 476 |
| 1 $nF$ | 114 → 100 | 12 | 500 $\mu s$ | 910 → 476 |
| 10 $nF$ | 114 → 100 | 3 | 2 $ms$ | 910 → 476 |
| 100 $nF$ | 114 → 100 | $\ll 1$ | 20 $ms$ | 910 → 476 |

**Table 4.14.:** Measurement results of stabilization methods for the robustness and reliability of charge pumps.

### 4.5.4 Discussion

Both feedback regulation methods to stabilize output voltages of high voltage charge pump against changes of operating conditions such as load and temperature variations are proven to be effective. All the ICs adopted in the test circuits are low voltage, whose functions can be easily realized on-chip and further optimized with relatively small chip areas.

The feedback regulation by adjusting the DC power supply shows better stabilization performance compared with the one by adjusting clock frequency, mainly due to the instability of the clock frequency generated by the adopted voltage controlled oscillator. Ideally, both methods should provide the similar voltage regulation performance. By using more accurate and stable voltage controlled oscillators, output voltages of charge pumps can be more effectively stabilized. The low voltage charge pump varies the available DC power supply for the stabilization of output voltages and consumes alone significant power and large layout area. In contrast, voltage controlled oscillators are usually small in the chip layout and show very low power consumption. However, it is more complex to design an accurate and stable voltage controlled oscillator compared with a low voltage charge pump. This leads to a better regulation using the low voltage charge pump with the same design effort. Tradeoffs between the regulation of the output voltage and required power consumption (or chip size) should be made, when feedback regulation methods are introduced.

Large output capacitors can considerably smooth the output voltage waveform. However, the recovery time of the charge pump becomes longer, which is normally not desired in high speed applications. Furthermore, capacitors of high values are extremely large in the chip layout. Those capacitors are usually supposed to be off-chip. ESD diodes can provide protection for charge pump circuits from high output voltages exceeding the maximum allowed limits. They are usually parasitic diodes and already included in the I/O cells. Therefore, they usually play a secondary role in integrated high voltage charge pumps.

## 4.6 Approaches to Increase Levels of Integration

Portable devices with low battery voltages feature an increasing number of complex SoCs which require high supply voltages. The integration level of high voltage generators with significant chip area in SoCs determines the overall layout size and functionalities of SoCs. With reduced chip area of those integrated high voltage generators, more circuit blocks of various functionalities can be implemented on-chip. Based on the two high voltage ASICs "Achilles" and "Balios" in Section 4.2 and 4.3, different approaches towards a higher level of integration can be investigated.

The proposed 4-phase charge pump architecture in Figure 4.5 from Section 4.1.4 belongs to improved variations of Pelliconi charge pump [PR03], whose output voltage can be calculated according to Equation 4.4 in Section 4.1.2. This equation shows that the output voltage $V_{out}$ of circuits based on Pelliconi charge pump is a function of clock frequency $f$, stage number $n$, pumping capacitor $C$ and its parasitic capacitor $C_s$. The voltage levels of the DC power supply $V_{dd}$ and clock signal $V_{clk}$ are considered as given operating conditions. Any increase of $V_{dd}$ and $V_{clk}$ considering the breakdown voltages of the adopted isolated low voltage devices requires additional circuits, which leads to even larger layout size. Therefore, the influence of $V_{dd}$ and $V_{clk}$ on the integration level is not discussed. The load current $I_L$ depends on the given load conditions which does not belong to the design parameters. The related design parameters to achieve a more compact chip layout are then clock frequency $f$, stage number $n$ and pumping capacitor $C$. For the same output voltage $V_{out}$ of the charge pump, smaller pumping capacitors $C$ are required at higher clock frequency $f$, when the stage number $n$ is fixed. Since high voltage capacitors occupy mostly large layout size, the overall layout size of the circuit will be reduced due to smaller layout area of high voltage capacitors at increased clock frequencies. Although it is also possible to increase the stage number $n$ instead of the clock frequency $f$ to generate the same output voltage $V_{out}$ with decreased pumping capacior values, the interconnections between stages will increase, which results in larger layout size as well. Besides, with higher stage number, the power efficiency of the circuit becomes lower because of the switching and conduction loss at the additional stages. Therefore, the increase of the clock frequency $f$ is the most effective method to approach a higher level of integration for high voltage charge pumps.

Beside the clock frequency $f$ which optimizes the layout size of the charge pump itself, other design factors such as the clock driver and the chosen technology play also an important role. Charge pumps usually need sufficient current supplies as charge sources for their charge transfer operation. Therefore, they require powerful clock drivers with high channel width which occupy also large layout size. The optimization of the on-chip clock drivers is then very helpful to reduce the chip area. Technologies with different feature sizes and process characteristics can further improve the integration level, which may increase the complexity of the design and require higher production costs.

### 4.6.1 Clock Frequency

The two high voltage ASICs "Achilles" and "Balios" are good examples to demonstrate the advantage of increasing the clock frequency to achieve higher integration levels. Using a clock frequency of $20\,MHz$ instead of the $10\,MHz$ used by "Achilles", "Balios" is able to generate slightly higher output voltages with the approximately 36 % reduction of the chip area compared with "Achilles". This is achieved by means of the decrease of the pumping capacitor values at each stage from $20\,pF$ ("Achilles") to $10\,pF$ ("Balios"). This benefit can be illustrated in Figure 4.41, where a comparison among concrete circuits using the high voltage CMOS technology H35 is given. The proposed 4-phase charge pump architecture and clock scheme shown in Figure 4.5 and 4.6 from Section 4.1.4 were adopted in the post-layout simulations for the comparison. All the dead times were of reasonable durations considering the related operating frequencies. Because high voltage capacitors (CPM of H35 for this comparison) are usually composed of capacitor arrays, their capacitor values are discrete. It is only possible to generate similar output voltages (approximately $110\,V$) at the same load conditions ($1\,M\Omega$, $30\,pF$) by using different pumping capacitor values. It can be seen in Figure 4.41 that the single stage of the circuit using a clock frequency of $100\,MHz$ needs the smallest layout size due to its significantly reduced layout size of capacitors, while the single stage layout of the circuit using $10\,MHz$ is the largest. A numerical description about the layout sizes of those single stages can be found in Table 4.15. The required higher stage number to achieve approximately $110\,V$ at higher clock frequencies is mainly due to the increased switching loss at the CMOS switches and the

parasitic capacitors of the pumping capacitors. Through the comparison discussed above, the clock frequency is proven to be the most effective design parameter to increase the level of integration of charge pump circuits.

| $f_{clk}(MHz)$ | **Layout Area($\mu m^2$)** | **Stage Number $n$ to achieve approximately 110 $V$** |
|---|---|---|
| 10 | 357504 | 36 |
| 20 | 184386 | 36 |
| 50 | 96900 | 38 |
| 100 | 63656 | 40 |

**Table 4.15.:** Layout areas of different single stages.

Nevertheless, there is a technological limitation regarding the increase of clock frequencies or the reduction of pumping capacitor values. Pumping capacitors must provide the control voltages for the CMOS switches in charge pumps. The gate capacitance at each CMOS switch is normally several hundred femtofarad. This indicates that too small pumping capacitors are not able to charge and discharge those parasitic gate capacitors of the CMOS switches (switch on and off those CMOS switches) effectively. Therefore, the increase of the clock frequency for higher integration level can only be applied where the reduced pumping capacitor values are still sufficient to control the CMOS switches in the circuit.

Furthermore, the rising and falling time of analog signals at voltage levels above $2\,V$ can be hardly minimized to less than $1\,ns$. At very high clock frequencies such as $100\,MHz$, the multiphase clock schemes may be difficult to be implemented.

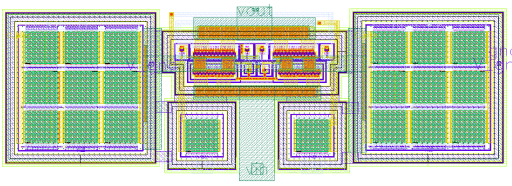
### 4.6.2 Clock Driver

The clock drivers in charge pumps should be strong enough to offer adequate currents to all the pumping capacitors. Especially in circuit architectures such as Pelliconi and Dickson charge pump, the most charge comes from the clock drivers through the pumping capacitors to the load. This implies if more stages are added, or the capacitor values of the pumping capacitors are increased, more charge will be required to be transferred from the clock drivers to the charge pump during each half clock period. Small clock drivers can reduce the stage voltage gain due to the considerable voltage drops over the small transistors with high on-resistance compared to those large transistors in large clock buffers. Furthermore, if high load currents exist at the output of the charge pump, small clock buffers will not be able to provide such additional high currents beside the currents to charge the pumping capacitors. Therefore, powerful clock drivers with transistors of high channel width are desired in charge pumps as high voltage generators with a high stage number and considerable load currents.

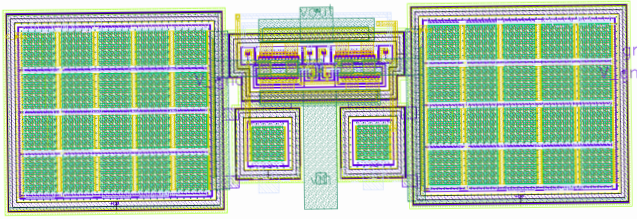
The layout area of those large clock drivers are usually significant. For example, in the high voltage ASIC "Achilles" using 4-phase clock schemes, each external clock signal is inputted to its on-chip clock drivers. $Clk_a$ and $Clk_b$ are mostly responsible for the charge transfer of the whole charge pump, so their on-chip clock drivers are extremely large, approximately $1.71 \times 0.56 = 0.9576\,mm^2$, respectively. $Clk_c$ and $Clk_d$ are not related to the charge transfer but to the control signals of the PMOS switches. Therefore, they need only small clock drivers of approximately $0.55 \times 0.23 = 0.1265\,mm^2$, respectively (see Figure 4.42). Wide metal layers for power and ground connections of those clock drivers are necessary to avoid the electromigration and to reduce the interconnection resistance between those clock drivers and the charge pump. If the layout areas of all those 4 clock drivers are summed up, it can be seen that they occupy a whole layout area of $2.1682\,mm^2$, nearly 10 % of the chip area of "Achilles".

Since large clock drivers are usually necessary in high voltage charge pumps, they should be designed carefully to fulfill the voltage and current requirements with optimized transistor sizes

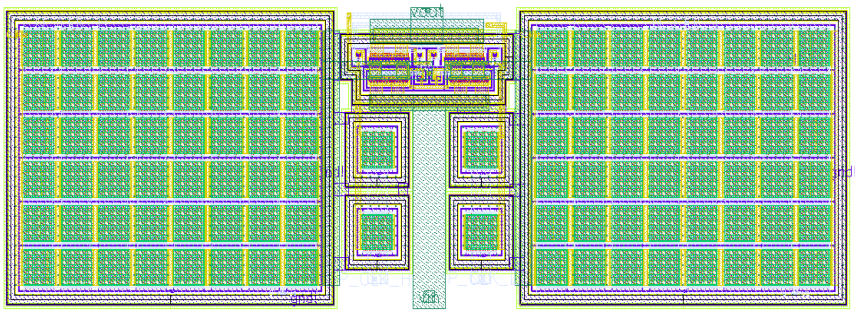
a) f = 100 MHz, $C_{pump}$ = 1 pF



b) f = 50 MHz, $C_{pump}$ = 2 pF



c) f = 20 MHz, $C_{pump}$ = 5 pF



d) f = 10 MHz, $C_{pump}$ = 10 pF

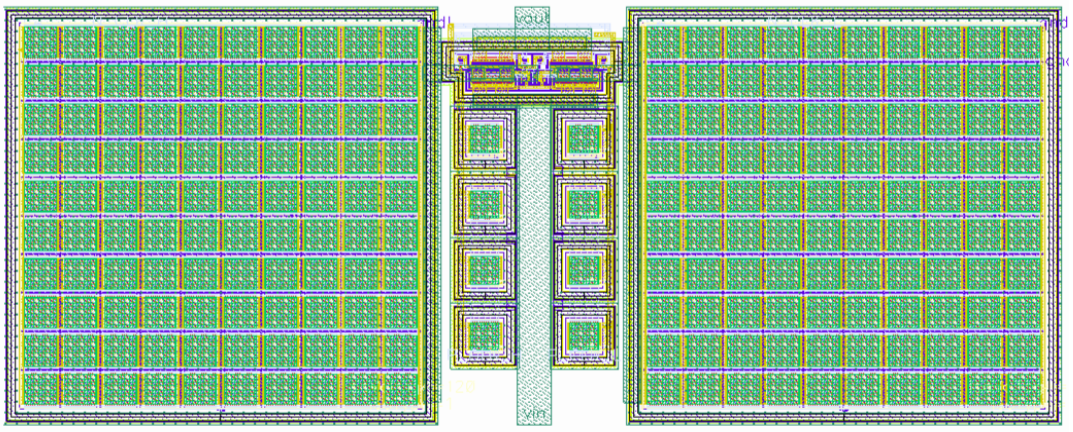
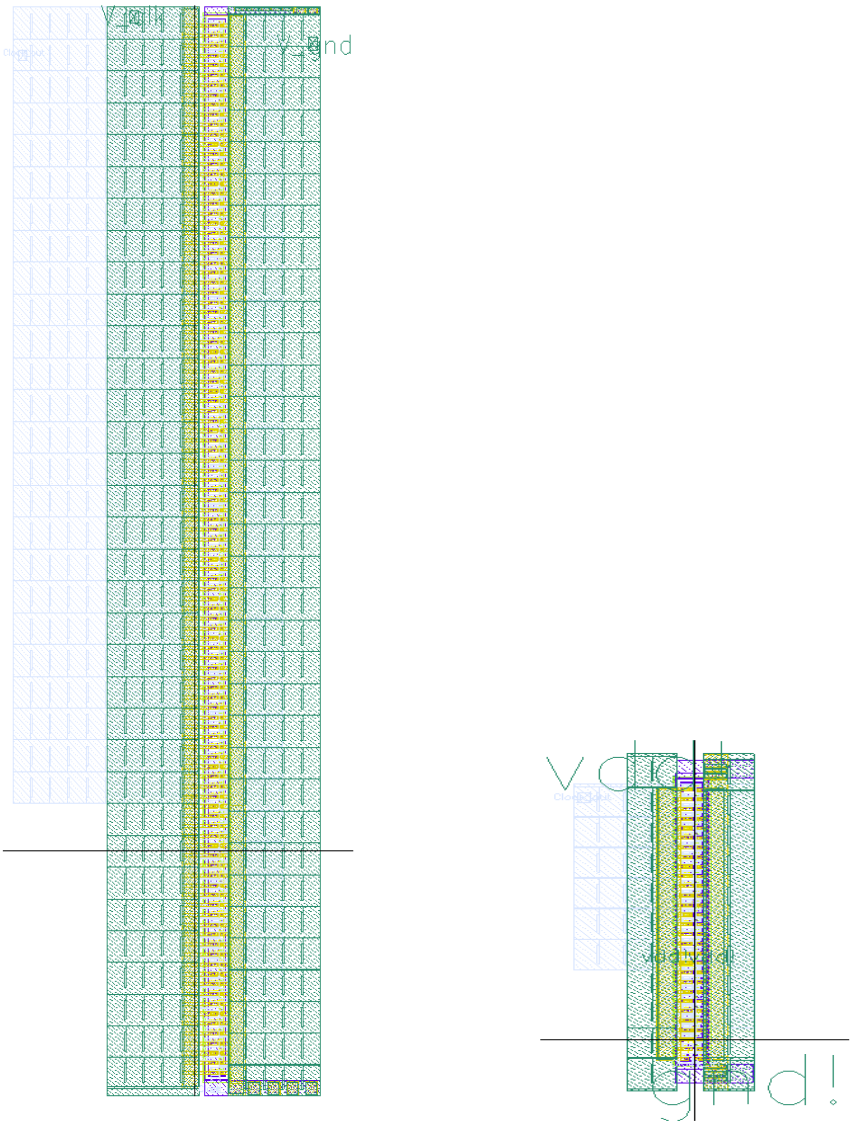


**Figure 4.41.:** Layouts of single stages of the proposed 4-phase charge pump architecture at various clock frequencies.

and layout areas. Clock drivers with excessively large size should be avoided. The optimization of transistor sizes at the tapered inverter chains is very helpful to achieve a more compact layout size.



a) Clock driver for CLKa or CLKb

b) Clock driver for CLKc or CLKd

**Figure 4.42.:** Layouts of the clock drivers in "Achilles".

### 4.6.3 Technology

The chosen technology for the implementation of high voltage charge pumps has also an important impact on the integration level. CMOS technologies with smaller feature sizes enable commonly more compact chip layouts. However, the selection of suitable technologies is dependent mainly on the maximum operating voltages of the circuit. Smaller technology dimensions indicate usually also lower maximum operating voltages. At the moment, 0.35 $\mu m$ high voltage CMOS technologies can operate up to 120 $V$, while 0.18 $\mu m$ ones are mostly only reliable until 50 $V$ [Dat14c; Dat14g].

During the miniaturization of the technology, physical effects such as oxide breakdown, electromigration, drift region in LDMOS and deep NWELL in the p-substrate become more significant. Therefore, the development of high voltage CMOS technologies with even smaller feature sizes but higher operating voltages is slowed down by the difficulties to solve those physical effects. Alternatively, other advanced technologies such as SOI technologies and 3D-integration gain in importance, when design requirements such as maximum operating voltages and maximum layout sizes can not be met by available high voltage CMOS technologies. By means of the vertical and horizontal isolation of dielectric, SOI technologies are able to provide much higher breakdown voltages of devices and less leakage current into the p-substrate compared to CMOS ones.

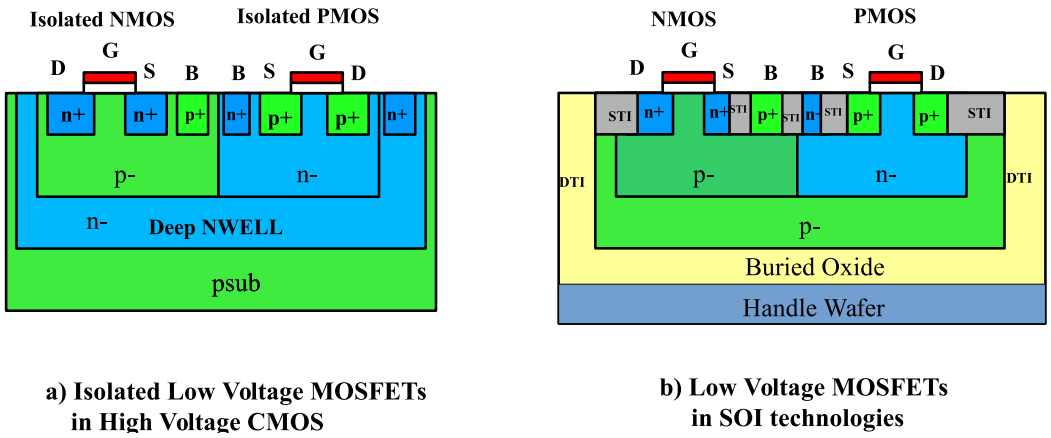



**Figure 4.43.:** Simplified cross sections of isolated low voltage transistors in CMOS technologies and low voltage transistors in SOI technologies.

Figure 4.43 illustrates simplified cross sections of isolated low voltage transistors in CMOS technologies and low voltage transistors in SOI technologies. It can be seen that both of them have similar electrical characteristics laterally and vertically. The deep NWELL and BOX (Buried Oxide) layer increase the vertical breakdown voltage of the devices in CMOS and SOI technologies, respectively. The lateral pn-isolation and DTI (Deep Trench Isolation) are responsible for the lateral breakdown voltages. (STI (Shallow Trench Isolation) is for the lateral isolation inside the device using SOI technologies.) Since oxide layer can withstand higher breakdown voltages, the maximum allowed operating voltages of SOI technologies are usually higher than those of CMOS ones. The high voltage CMOS technology H18 of AMS ($0.18\,\mu m$, $50\,V$) and SOI technology XT018 of Xfab ($0.18\,\mu m$, $200\,V$) are good examples for the comparison [Dat14b; Dat14f]. Moreover, the DTI in SOI technologies requires smaller layout size than the pn-isolation in CMOS technologies. Transistors in SOI technologies have usually more compact layout sizes than those in CMOS technologies with the same technology dimension. However, the capacitance density of high voltage capacitors in both high voltage CMOS and SOI technologies is similar. It indicates that if the most part of the chip area is occupied by high voltage capacitors, the overall chip area will not be significantly reduced by using SOI technologies instead of CMOS technologies [Dat14b; Dat14f]. Due to the characteristics of the low voltage transistors in SOI technologies, the 4-phase charge pump architectures proposed in Section 4.1.4 can be directly applied in SOI technologies. All the adopted isolated low voltage transistors in high voltage CMOS technologies can be replaced by those low voltage transistors in SOI technologies. However, SOI technologies need higher production costs in comparison with CMOS ones, which sometimes limits their applications.

When the overall chip layout of the circuit is too large and no longer reasonable to be monolithically integrated, 3D-integration shows an effective way to achieve an acceptable footprint of the circuit [XCS10]. In 3D-integration, two or more stacked chips can be connected by means of TSV (Through Silicon Vias), for example. Figure 4.44 shows a possible 3D-integration concept, when the high voltage capacitors in charge pumps can not be integrated with the switches together due to their large layout sizes. The footprint of these two stacked chip is much smaller than a monolithically integrated one. Furthermore, these two chips can be fabricated in different technologies, so that optimized performance of devices can be achieved. The discussed heap charge pump architecture in Figure 4.3 from Section 4.1.3 is not suitable for the monolithic integration, since it needs very large pumping capacitors to overcome the significant gain reduction caused by parasitic capacitors and high load currents, which makes this architecture only applicable in discrete circuits. Using 3D-integration, it is possible to implement this architecture in the form of integrated circuits. Nevertheless, the introduction of TSV in 3D-integration brings also more interconnection loss and parasitics. Generally, the influences of 3D-integration on the electrical, thermal and mechanical characteristics of the circuit should be investigated extensively. Besides, interconnections such as TSV introduced for the 3D-integration occupy also a large chip area which should be considered.

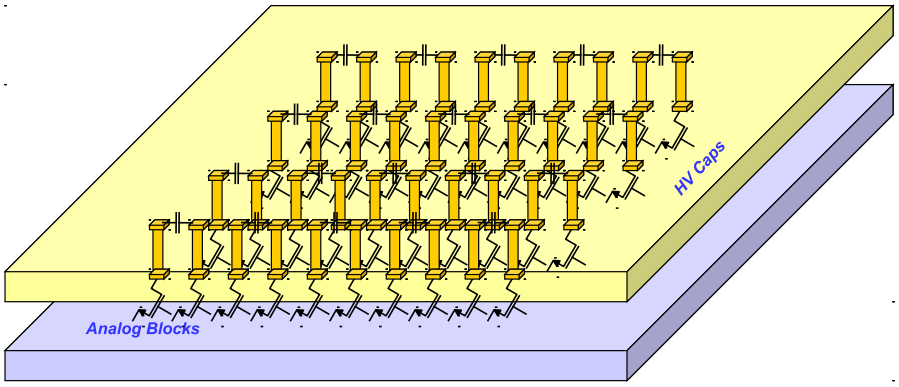



**Figure 4.44.:** 3D-integration by means of TSV (Through Silicon Vias).

## 4.7 Limitations of CMOS Technologies for Negative High Voltage Generation

The 4-phase charge pump architectures proposed in Section 4.1.4 are intended mainly for positive high voltage generation. By connecting the output to the round and changing the input to the output compared with Figure 4.8, the proposed architectures can principally also generate negative high voltages (see Figure 4.45). However, CMOS technologies have certain limitations which make it difficult to generate negative voltages lower than certain voltage levels by using charge pumps.

### 4.7.1 Technological Limitations

In conventional bulk CMOS technologies, it is impossible to adopt charge pump circuits to generate negative voltages, when NMOS transistors are necessary parts. This is because the p-substrate normally must be biased to the lowest voltage level in the whole chip, which is usually the ground. NMOS transistors in bulk CMOS technologies are realized directly in the p-substrate. Therefore, each terminal of those NMOS transistors can be biased at negative voltage levels. Otherwise the

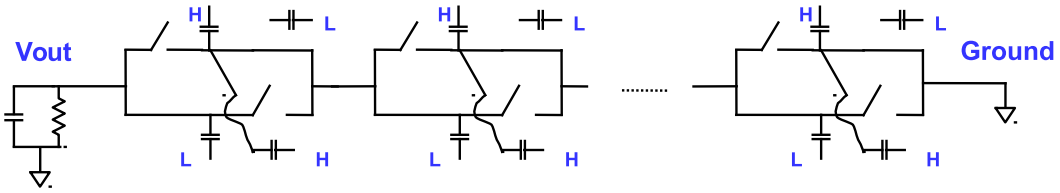



**Figure 4.45.:** Multistage proposed 4-phase charge pump for negative high voltage generation.

pn-junction between the p-substrate and n-doped area below NMOS terminals will conduct. PMOS transistors in bulk CMOS technologies can have negative terminal voltages due to their triple-well structures. Similarly, isolated NMOS transistors can also be applied in negative voltage applications due to the introduced (deep) NWELL. However, the pn-junctions inside the (deep) NWELL in isolated low voltage transistors are low voltage diodes which have only very low breakdown voltages ($< 10\,V$). Figure 4.46 shows all the pn-junctions inside the introduced (deep) NWELL. Only when the (deep) NWELL is biased by voltage levels higher than that at the p-substrate, then the pn-junctions in the (deep) NWELL can be biased by negative voltages below their reverse breakdown voltages. Otherwise, the forward conduction of some pn-junctions may occur, which leads to the malfunction or even damage of the device. In [YIN09], a negative voltage charge pump based on Dickson charge pump is presented, which adopts only PMOS transistors without special triple-well processes and is able to generate up to -6 $V$ negative output voltages. For circuits like Pelliconi charge pump, NMOS transistors are usually indispensable, so triple-well CMOS processes must be employed. In [YIN09], a negative voltage charge pump based on Pelliconi charge pump is also demonstrated, which can generate maximum -9 $V$ negative output voltages. It can be seen that even with isolated low voltage transistors in triple-well CMOS processes, it is difficult to generate negative voltages lower than -9 $V$ by using charge pumps, mainly due to the low reverse breakdown voltages of the pn-junctions inside the (deep) NWELL.

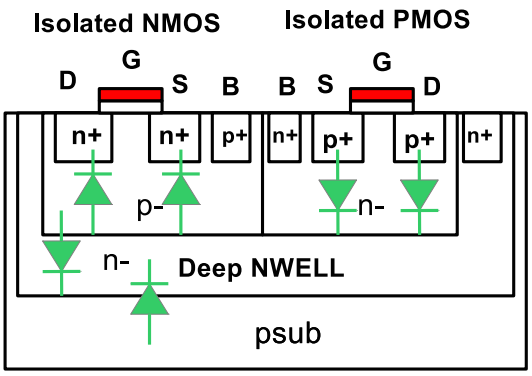



**Figure 4.46.:** Diodes in isolated low voltage transistors.

In order to generate lower negative output voltages, isolated high voltage transistors can be taken into account. The isolated high voltage PMOS transistors can be applied in the negative high voltage generation due to their pn-junctions with low doping concentration and long depletion zones, which result in high reverse breakdown voltages. The isolated high voltage NMOS transistors are not

suggested to be used in negative voltage applications, since their parasitic bipolar transistors in the p-substrate can get triggered, when those NMOS transistors are switched on and negative voltages are applied at the transistor terminals. In negative voltage applications, the isolated high voltage NMOS transistors are supposed to be always switched off for reliability reasons [Dat14c]. Furthermore, isolated high voltage transistors have connected Source and Bulk terminals and need large layout area. They are usually not suitable for charge pumps requiring a high number of transistors, for example, for the 4-phase charge pump architectures proposed in Section 4.1.4.

### 4.7.2 SOI Technologies as Alternative Solutions

As discussed in Section 4.6.3, SOI technologies can be a good alternative for high voltage CMOS technologies, when design requirements such as high maximum operating voltages can not be met. SOI technologies can be directly applied in negative high voltage applications due to their vertical and lateral dielectric isolation. The breakdown voltages of those vertical and lateral dielectric isolation layers can usually reach the maximum allowed operating voltage of the chosen technology without consideration of the voltage polarity. For instance, approximately -200 $V$ negative high voltage can be generated by a 63-stage proposed 4-phase charge pump from 3.7 $V$ DC power supply in the 0.18 $\mu m$ 200 $V$ SOI technology XT018 of Xfab (see Figure 4.47).

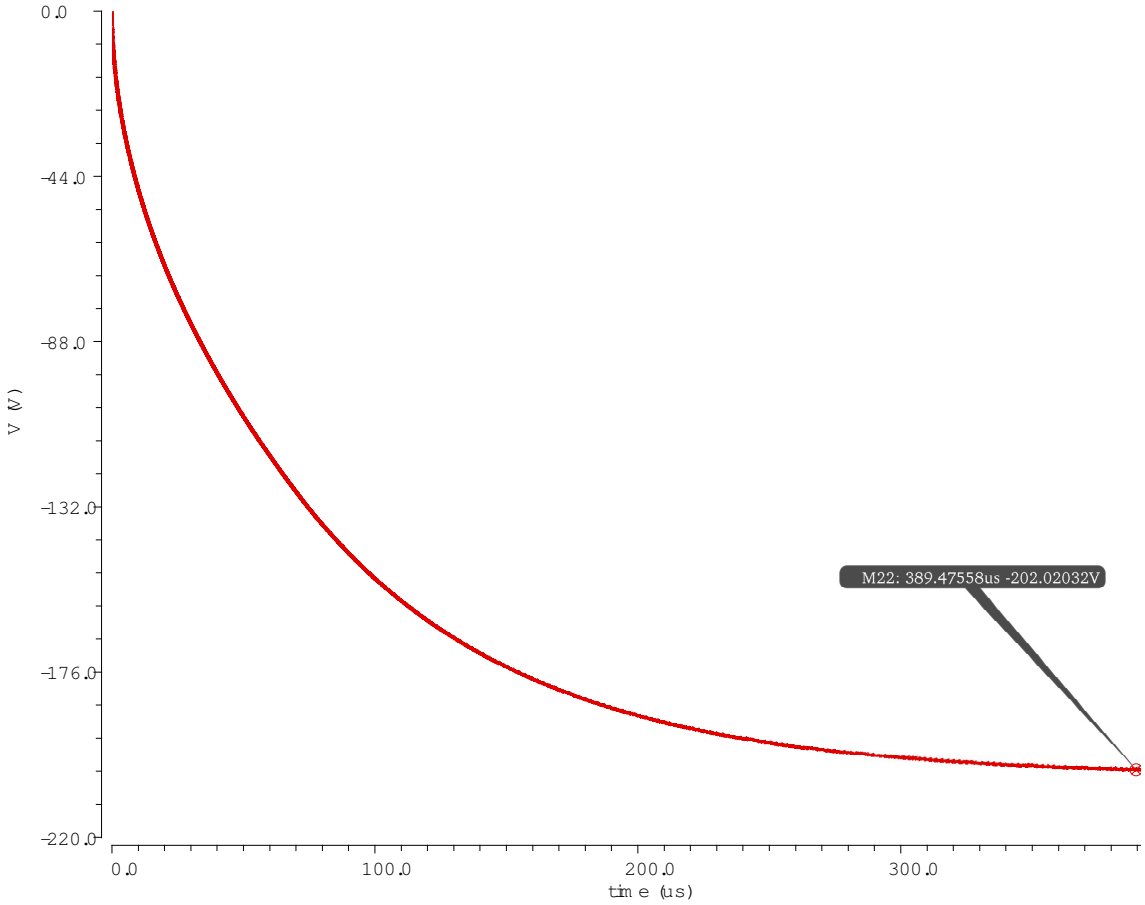



**Figure 4.47.:** Simulation result of the negative high output voltage of a 63-stage proposed 4-phase charge pump using XT018.

## 4.8 An Application Example: Reconfigurable Antenna Module with Integrated High Voltage Charge Pump and Digital Analog Converter

Modern devices for communication have to operate in many different frequency bands and with several standards (such as GSM, UMTS, LTE, WLAN etc.). The integration of all functionalities into one handheld device is getting more and more demanding in terms of system complexity and energy efficiency, since every standard and frequency band requires individual hardware functionality. In the LOEWE (Landes-Offensive zur Entwicklung Wissenschaftlich-ökonomischer Exzellenz) research priority program Cocoon (Cooperative sensor communication), a reconfigurable dualband antenna module for energy-efficient reconfigurable multiband RF transceivers in mobile applications was developed and demonstrated [com11; GR+14]. With this module, it is possible to achieve optimized power efficiency, hardware costs and footprint dimensions on PCBs.

Figure 4.48 illustrates the adopted architecture for the reconfigurable antenna module. The integrated high voltage charge pump "Balios" implemented in Section 4.3 plays a key role in the module, which generates a high DC voltage of 110 $V$ from the available 3.7 $V$ battery. This generated high DC voltage serves as the DC power supply voltage for the two 8-bit high voltage D/A (Digital/Analog) converters, whose output voltages $V_1$ and $V_2$ are controlled by their separate 8-bit input digital signals and can sweep from 0 $V$ to 110 $V$ independently by certain voltage steps [NH13]. In Figure 4.49, the mounted high voltage charge pump and D/A converter in their chip sockets are displayed. Since both ASICs use the same technology H35 of AMS for the fabrication, a further integration into a single chip can be realized.

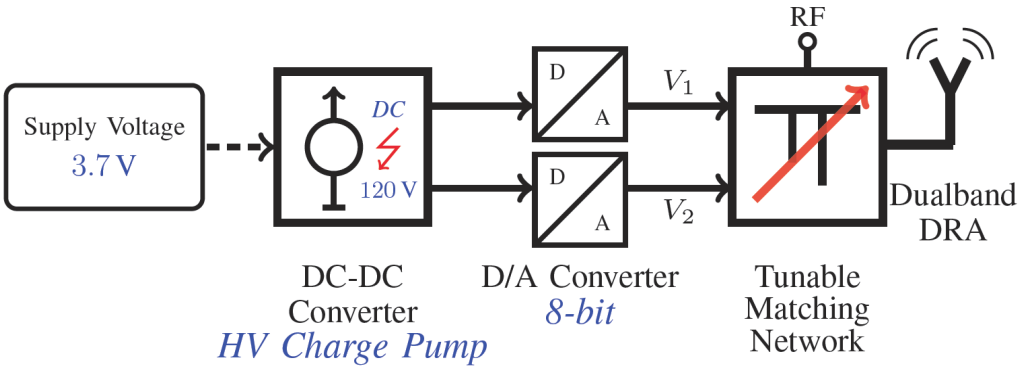



**Figure 4.48.:** Adopted architecture for the reconfigurable antenna module [GR+14].

Two BST (Barium-Strontium-Titanate) varactors, whose permittivity can be tuned by applying an external electrical field resulting in a tunable capacitance, is used to build the TMN (Tunable Matching Network). The high DC voltage $V_1$ and $V_2$ are applied as the necessary high bias voltages for the two BST varactors in the TMN, respectively (see Figure 4.50). The dualband DRA (Dielectric Resonator Antenna) is connected to the TMN for the signal transmission.

Measurement results in Figure 4.51 show that the input reflection $S_{11}$ of the TMN module can be minimized by choosing proper bias voltages $V_1$ and $V_2$. Lower input reflection $S_{11}$ of the TMN module indicates higher energy efficiency. The center frequency $f$ of the TMN module will be changed by the bias voltages $V_1$ and $V_2$, which are controlled by their 8-bit digital signals, respectively. These digital signals can be created according to certain optimized algorithms which analyze the current

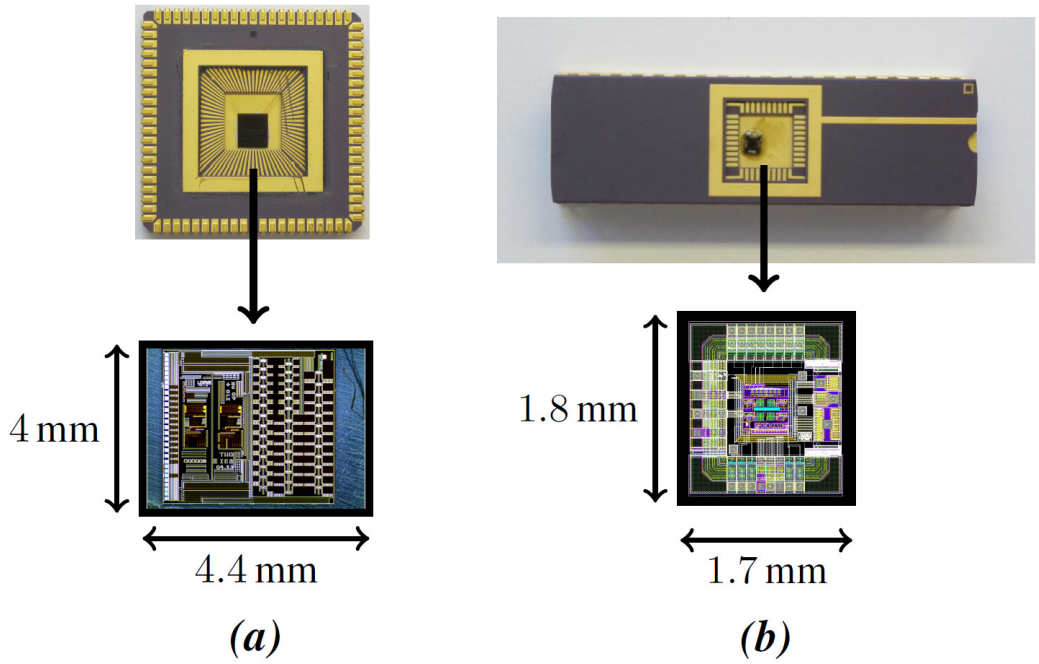



**Figure 4.49.:** Mounted ASICs in chip sockets at the demoboard (a) HV (High Voltage) charge pump and (b) D/A (Digital/Analog) converter [HSe12; GR+14; NH13].

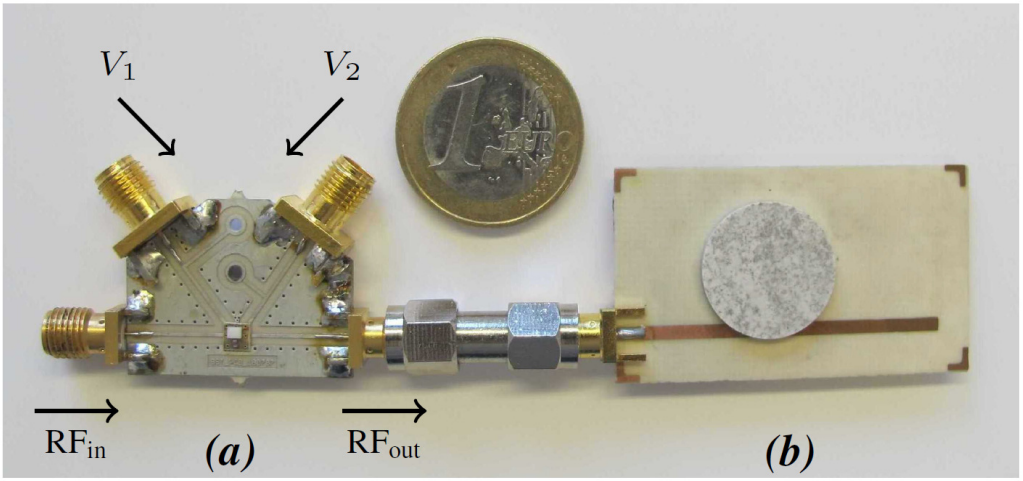



**Figure 4.50.:** Photograph of (a) TMN (Tunable Matching Network) module connected to a (b) dual-band DRA (Dielectric Resonator Antenna) [GR+12; GR+14].

environment and determine the current optimum center frequency $f$ of the TMN module resulting in the lowest $S_{11}$ [Zhe+08].

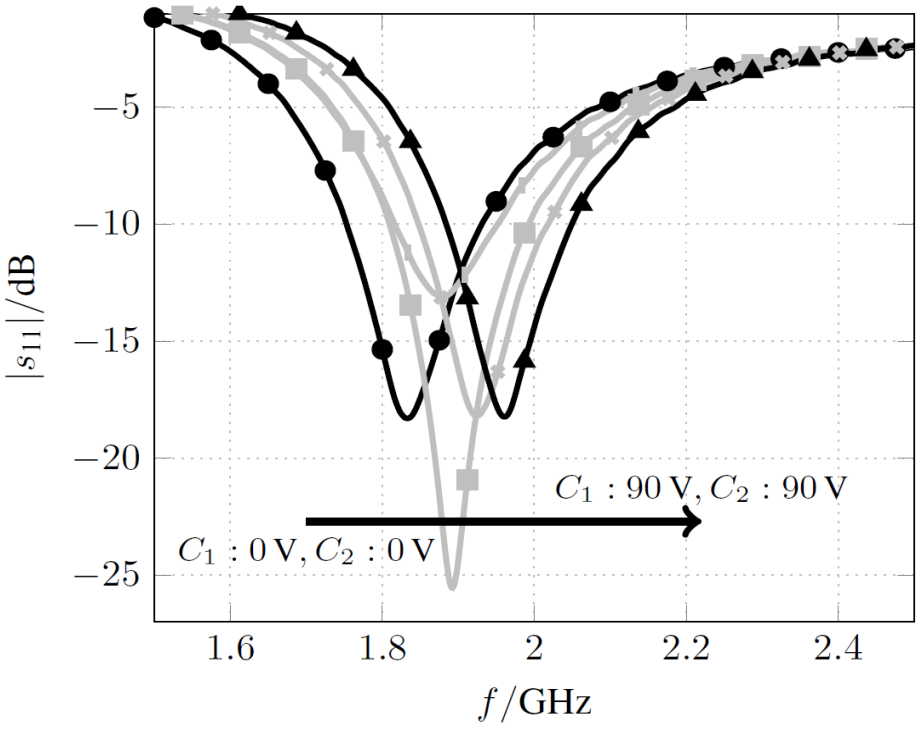



**Figure 4.51.:** Measured results of the TMN module for different capacitance values biased from 0 V to 90 V [GR+14].

A demonstrator of the reconfigurable antenna module which presents the concrete realization of the adopted architecture displayed in Figure 4.48 was implemented. The switches are used as the manual input of the two 8-bit digital signals for the two high voltage D/A converters, which can further be replaced by microcontrollers based on algorithms to determine the optimum center frequency of the TMN [Zhe+08]. Compared to boost converter with large inductors, the integrated high voltage charge pump provides the possibility to overcome integration constraints of high voltage generation into a portable device. Hence, the integration of reconfigurable RF frontends into handheld devices is proven to be feasible [GR+14].

## 4.9 Summary

This chapter presents the proposed 4-phase charge pump architectures using dead time techniques with high voltage gain and power efficiency in comparison with conventional charge pump architectures such as Dickson, Pelliconi and heap charge pump. The influences of high voltage capacitors in CMOS technologies are extensively investigated with respect to voltage gain and power efficiency of the charge pump. One of the proposed 4-phase charge pump architectures was successfully implemented in two high voltage ASICs with codename "Achilles" and "Balios". "Achilles" using an approximately 10 $MHz$ clock frequency with a total chip size of 21.84 $mm^2$ is the first fully integrated CMOS charge pump in literatures which is able to generate up to 120 $V$ from low DC supply voltages such as 3.7 $V$. "Balios" using an increased clock frequency of approximately 20 $MHz$ and providing the similar voltage performance to that of "Achilles" is a high voltage SoC with the on-chip clock generation, whose total chip size is about 17.6 $mm^2$. Other advanced clock schemes with dead time techniques are proposed and analyzed. The advantages of those clock schemes regarding the

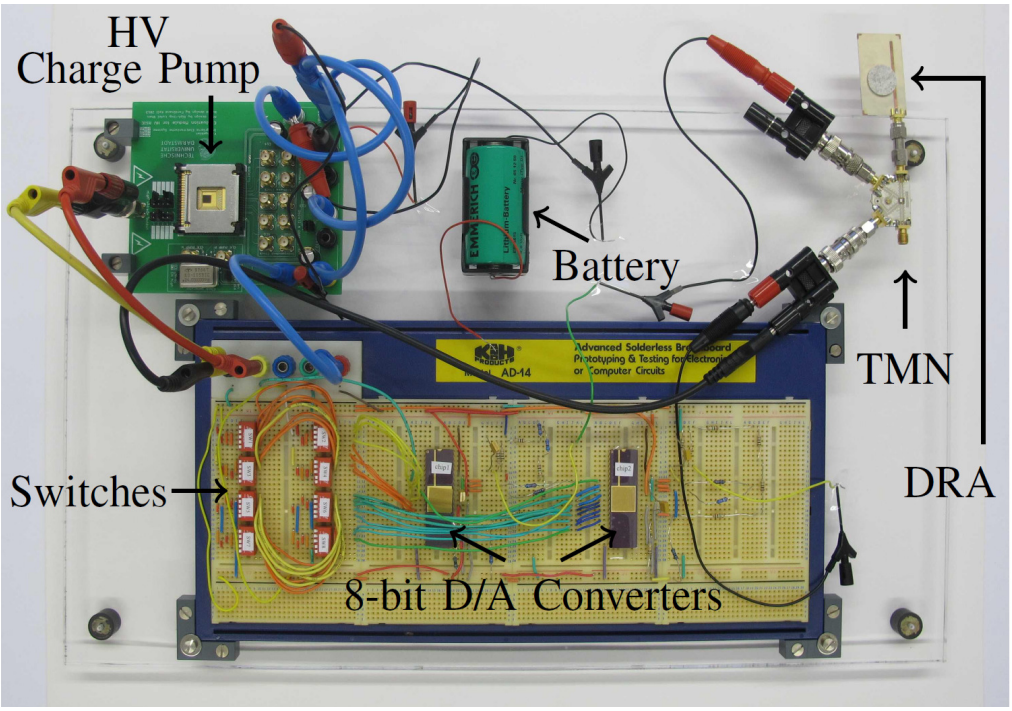



**Figure 4.52.:** Demoboard of the reconfigurable antenne module [GR+14].

reduction of the reverse currents in cascaded charge pump stages are proven by measurement results based on "Achilles". Several stabilization methods such as feedback regulation methods by adjusting the clock frequency, DC power supply voltage etc. to stabilize the output voltage of the charge pump are proposed. They are also proven by measurement results based on two discrete test circuits composed of "Balios" and other ICs, whose functionalities can be further integrated into "Balios". Several approaches to achieve higher integration levels of the charge pump are investigated, where the clock frequency is the most effective method to reduce the charge pump chip size due to the smaller required pumping capacitor values for the same output voltage. The technological limitations of CMOS technologies to generate negative high voltage is pointed out, which can be solved by using other technologies such as SOI technologies. At last, a concrete application example of fully integrated high voltage charge pumps is given to demonstrate the importance of an increased level of integration.

# 5 Conclusion and Outlook

## 5.1 Conclusion

Step-up DC-DC conversion to generate high DC voltages from low battery voltages in portable devices used to be mainly realized by partially integrated boost converter with external bulky inductors. Conventional charge pump architectures such as Dickson charge pump [Dic76] and Pelliconi charge pump [PR03] are more suitable in low voltage applications due to their drawbacks such as body effect, reverse currents, large voltage drops across diodes or diode-connected MOSFETs etc. This results in low voltage gain, low power efficiency and extremely large layout size for the on-chip high voltage generation. High voltage CMOS technologies matching BCD performance are cost-effective and reliable. They support the monolithic integration of step-up DC-DC converters. High voltage CMOS devices are usually modeled in a special way because of their complicated device structures and operating conditions under high voltage stresses in comparison to low voltage ones. SOAC is an indispensable part detecting the degradation or damage of high voltage devices during the simulation to ensure that all the devices always operate under their maximum allowed operating conditions. Moreover, layout techniques for high voltage CMOS ASICs with respect to devices, layers and ESD protection are beneficial to improve the feasibility and reliability of the circuit.

In this dissertation, an innovative 4-phase charge pump architecture to generate high voltages beyond $100\,V$ effectively and reliably for battery-powered mobile applications was proposed. It was successfully implemented by two fully integrated high voltage CMOS ASICs with codename "Achilles" and "Balios", respectively. Pelliconi charge pump was chosen as the basic circuit architecture because of its high voltage gain and high integration level compared to Dickson charge pump and boost converter. However, the reverse currents between cascaded stages and the conduction of the body diode in Pelliconi charge pump become significant in high voltage applications, which reduce the voltage gain and reliability of Pellicon charge pump as on-chip high voltage generators. The proposed 4-phase charge pump architecture based on Pelliconi charge pump adopts the dynamic bulk-biasing technique [Shi+00] to overcome the body effect problem as well as a 4-phase clock scheme with dead time techniques [WTK10] to reduce the reverse currents. Both techniques were commonly employed in low voltage applications only. With further optimization regarding circuit compactness and reliability, the proposed 4-phase charge pump architecture is able to generate up to the maximum operating voltage of the chosen CMOS technology. Since merely isolated low voltage high offset transistors instead of large-sized high voltage transistors are necessary to realize the MOS switches, the required layout area of the proposed 4-phase charge pump architecture is minimized. High voltage sandwich capacitors with large layout areas and parasitic capacitors are currently indispensable in high voltage CMOS ASICs. The influences of those high voltage capacitors on the voltage gain and power efficiency of high voltage charge pumps were extensively investigated. The configuration providing high voltage gain but low power efficiency was chosen for the implementation of those high voltage capacitors in the proposed 4-phase charge pump to reduce the overall layout size.

The first test chip "Achilles" was implemented in the $0.35\,\mu m$ high voltage CMOS technology H35 of AMS and occupies a total chip size of $21.84\,mm^2$. Therein, the charge pump captures $14.4\,mm^2$. "Achilles" is able to generate up to $120\,V$ output voltage from low voltage DC power supplies such as $3.7\,V$. The second chip "Balios" uses the same technology as "Achilles" equipped and provides a similar output voltage. However, the second chip is with additional circuit parts for the on-chip

4-phase clock generation. Compared to the first generation, "Balios" only occupies a chip size of $17.6\,mm^2$, wherein $9.2\,mm^2$ is covered by the charge pump. The reduction on the chip size is mainly due to the reduced layout areas of the pumping capacitors by the increased clock frequency. The measurement results of both high voltage ASICs confirm the proposed 4-phase charge pump architecture and clock scheme. They increase the voltage gain, integration level as well as reliability of the circuit in comparison with conventional charge pump architectures and 2-phase non-overlapping clock schemes.

Furthermore, variations of the proposed 4-phase charge pump architecture using only PMOS switches or enhanced controlling of switches were also proposed and investigated. However, the proposed 4-phase charge pump architecture was proven by simulation results to be the best solution to achieve high voltage charge pumps with respect to compact layout size and high voltage gain. Further advanced 4-phase clock schemes with dead time techniques were proposed and verified by simulation as well as measurement results. They show increased voltage gain and power efficiency compared to the previously proposed 4-phase clock scheme. However, the complexity of those clock schemes increases the difficulty of the clock generation and distribution. Several stabilization methods were proposed to stabilize the output voltage and to improve the reliability of high voltage charge pumps against operating condition variations. These methods include feedback regulation, stabilizing diodes and capacitors and were proven by the measurement results based on "Balios". They can easily be further integrated on-chip because they are mostly composed of standard analog blocks. Furthermore, an extensive study on the approaches to increase the integration levels of high voltage CMOS charge pumps was made. It is concluded that the clock frequency is the most effective design parameter to achieve high integration levels. By increasing the clock frequency, the necessary capacitance value of the pumping capacitors, which usually occupy dominant chip areas, will be reduced. Therefore, the required chip area is minimized. However, in order to overcome the limitations of CMOS technologies in negative high voltage generation, SOI technologies are considered as an alternative solution.

According to the obtained design experience in integrated high voltage CMOS charge pumps, a comprehensive design strategy regarding CMOS high voltage generators was proposed. It covers important aspects such as System-on-Chip or System-in-Package, architecture and device selection, trade-offs among various design requirements, control circuits, clock generation and distribution as well as challenges during circuit simulations. Besides, main contribution was provided to the proposed design flow for high voltage CMOS ASICs [Hof+13], which focuses mainly on the feasibility and reliability. The proposed design strategy and design flow are intended to help designers improving their design techniques in fully integrated high voltage charge pumps.

In this dissertation, simulation and experimental results prove that charge pump architectures for high voltage generation are able to be monolithically implemented in high voltage CMOS technologies. By adopting innovative charge pump architectures using advanced techniques such as dynamic bulk-biasing technique and 4-phase clock schemes with dead time techniques, the integration level of high voltage CMOS charge pumps can be significantly increased. Using highly integrated high voltage charge pumps for the on-chip high voltage generation, further functionalities such as on-chip clock generation, feedback regulation etc. are feasible options for high voltage SoCs with reasonable chip sizes and stable voltage performance. By means of optimization of design parameters such as the clock frequency, two high voltage ASICs "Achilles" and "Balios" adopting the proposed 4-phase charge pump architecture were implemented in a typical $120\,V$ high voltage CMOS technology. Both fully integrated ASICs are able to generate up to $120\,V$ DC voltages with high voltage gain. They show the best performance of high voltage generation among all the integrated high voltage charge pumps [Dou10; EAS13].

## 5.2 Outlook

With the knowledge of the monolithic integration of CMOS high voltage charge pumps, future work can focus on improvements of voltage performance, power efficiency, footprint on PCBs and reconfigurability. Based on the successfully implemented high voltage ASICs "Achilles" and "Balios", fully integrated high voltage charge pumps can be optimized by using the following methods:

- **On-chip feedback regulation:** To obtain high stability of output voltage against the variations of operating conditions, feedback regulation was investigated in Section 4.5.1. This includes an adjustment of the clock frequency and DC power supply. These feedback regulation methods were used to stabilize the output voltage of "Balios". However, they were implemented with discrete components. Nevertheless, those standard low voltage analog circuits can be integrated on-chip due to their in general small layout sizes. In this way, monolithic high voltage charge pumps with stabilized output voltages can be realized. Besides, the integrated feedback circuits are supposed to be more accurate and effective than discrete ones due to the reduced interconnection losses and parasitics.

- **Charge recycling:** The power efficiency of the two high voltage ASICs is only about 10 % and therefore relatively low. The considerable waste of charge arise from the charging and discharging of the parasitic capacitors of the pumping capacitors delivered by the clock drivers. In [Dou10], a charge recycling method is proposed which prevents the charge stored at the parasitic capacitors from flowing back to ground. Instead, it is reused to charge the pumping capacitors of neighboring stages. Hence, the power efficiency is increased. Since all the related parasitic capacitors locate at the low voltage parts of the circuit, standard low voltage circuits and clock schemes can be adopted to realize the charge recycling with reasonable chip areas.

- **3D-integration:** It is already introduced in Section 4.6.3 and considered to be an effective method to obtain small footprint on PCBs, when the chip size can not be minimized to an acceptable level in CMOS technologies. The chip sizes of both "Achilles" and "Balios" are dominated by the high voltage capacitors. In future, high voltage capacitors and other circuit components of the charge pump can be realized in two different chips. The stacked chips using 3D-integration will require very small footprint. With increased clock frequency and hence reduced capacitor areas, the reduction of the footprint will be even more significant.

- **Programmable voltage reference:** The proposed 4-phase charge pump architecture does not show any reconfigurability. If the operating conditions such as the DC power supply, clock frequency and load current are fixed, the output voltage of charge pumps using the proposed architecture is constant. Therefore, the programmable voltage reference with the help of the feedback regulation discussed in Section 4.5.1 is a promising approach to realize the reconfigurability. Consequently, it is possible to adjust output voltages of the charge pump to certain voltage levels by changing the voltage level of the programmable voltage reference in the feedback circuit.

By means of these methods, fully integrated high voltage CMOS charge pumps with improved circuit performance and extended functionalities could be realized, which enable more complex high voltage SoCs.

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# A Device Parameters and Layout of a Single Stage of "Achilles"

| Device | Type | Channel Width ($\mu m$) | Channel Length ($\mu m$) | Capacitor Value ($pF$) |
|---|---|---|---|---|
| M1 | NMOSIM | 24 | 0.5 | - |
| M2 | NMOSIM | 24 | 0.5 | - |
| M3 | PMOSIM | 36 | 0.5 | - |
| M4 | PMOSIM | 36 | 0.5 | - |
| M5 | NMOSIM | 1 | 0.5 | - |
| M6 | NMOSIM | 1 | 0.5 | - |
| M7 | PMOSIM | 3 | 0.5 | - |
| M8 | PMOSIM | 3 | 0.5 | - |
| M9 | PMOSIM | 3 | 0.5 | - |
| M10 | PMOSIM | 3 | 0.5 | - |
| C1 | CWPM | - | - | 10.747 |
| C2 | CWPM | - | - | 10.747 |
| C3 | CWPM | - | - | 0.313 |
| C4 | CWPM | - | - | 0.313 |

**Table A.1.:** Device parameters of a single stage proposed 4-phase charge pump with CWPM in "Achilles".

| Device | Type | Channel Width ($\mu m$) | Channel Length ($\mu m$) | Capacitor Value ($pF$) |
|---|---|---|---|---|
| M1 | NMOSIM | 24 | 0.5 | - |
| M2 | NMOSIM | 24 | 0.5 | - |
| M3 | PMOSIM | 36 | 0.5 | - |
| M4 | PMOSIM | 36 | 0.5 | - |
| M5 | NMOSIM | 1 | 0.5 | - |
| M6 | NMOSIM | 1 | 0.5 | - |
| M7 | PMOSIM | 3 | 0.5 | - |
| M8 | PMOSIM | 3 | 0.5 | - |
| M9 | PMOSIM | 3 | 0.5 | - |
| M10 | PMOSIM | 3 | 0.5 | - |
| C1 | CPM | - | - | 10.819 |
| C2 | CPM | - | - | 10.819 |
| C3 | CPM | - | - | 0.348 |
| C4 | CPM | - | - | 0.348 |

**Table A.2.:** Device parameters of a single stage proposed 4-phase charge pump with CPM in "Achilles".

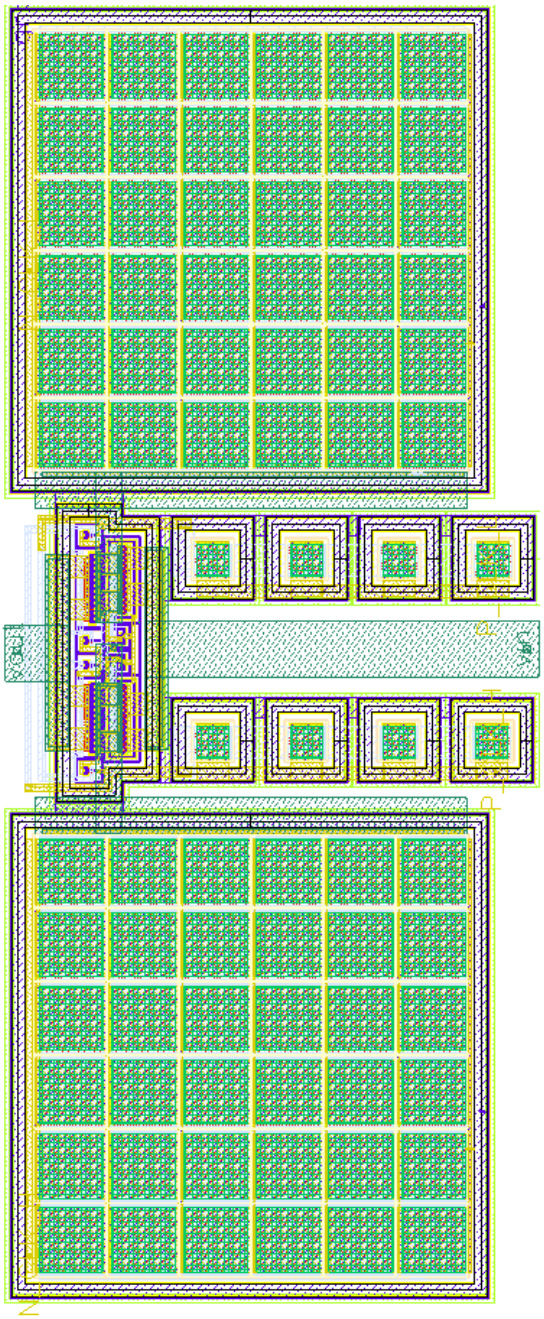

**Figure A.1.:** Layout of a single stage proposed 4-phase charge pump with CWPM in "Achilles".

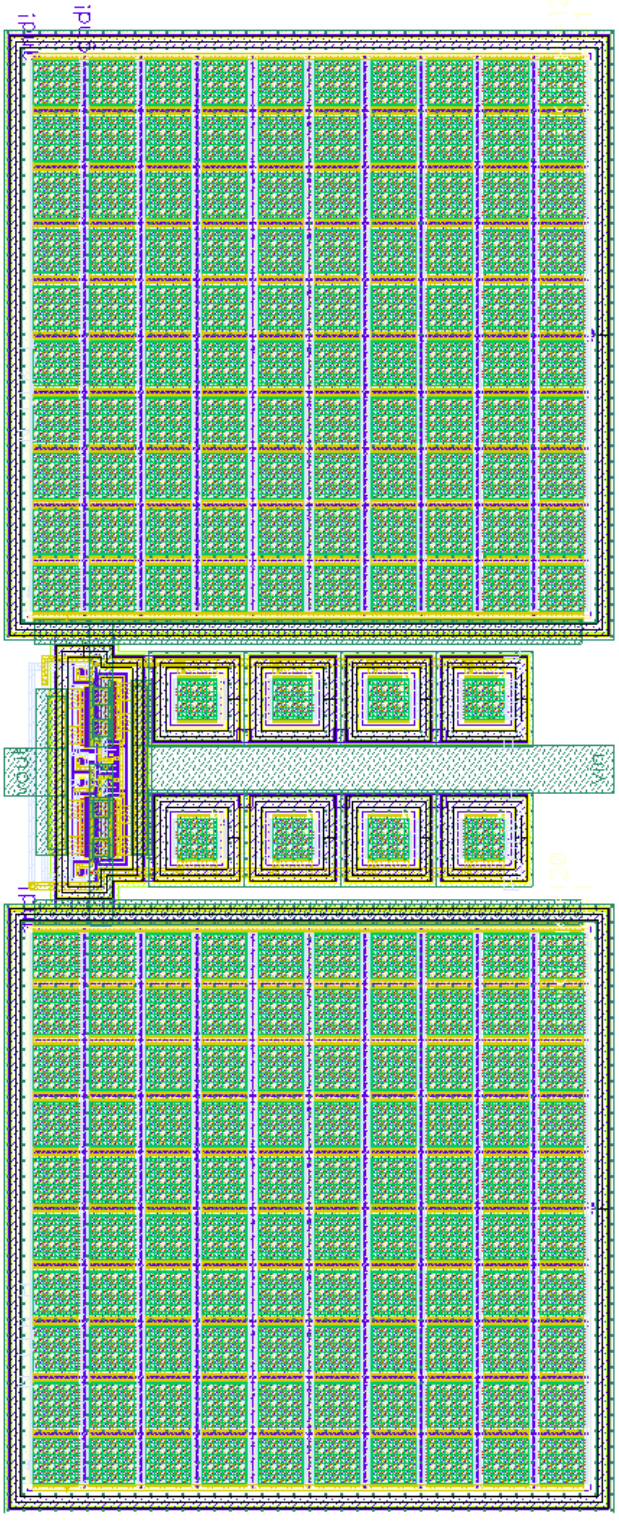

**Figure A.2.:** Layout of a single stage proposed 4-phase charge pump with CPM in "Achilles".

# B Device Parameters and Layout of a Single Stage of "Balios"

| Device | Type | Channel Width ($\mu m$) | Channel Length ($\mu m$) | Capacitor Value ($pF$) |
|---|---|---|---|---|
| M1 | NMOSIM | 24 | 0.5 | - |
| M2 | NMOSIM | 24 | 0.5 | - |
| M3 | PMOSIM | 36 | 0.5 | - |
| M4 | PMOSIM | 36 | 0.5 | - |
| M5 | NMOSIM | 1 | 0.5 | - |
| M6 | NMOSIM | 1 | 0.5 | - |
| M7 | PMOSIM | 3 | 0.5 | - |
| M8 | PMOSIM | 3 | 0.5 | - |
| M9 | PMOSIM | 3 | 0.5 | - |
| M10 | PMOSIM | 3 | 0.5 | - |
| C1 | CWPM | - | - | 4.776 |
| C2 | CWPM | - | - | 4.776 |
| C3 | CWPM | - | - | 0.156 |
| C4 | CWPM | - | - | 0.156 |

**Table B.1.:** Device parameters of a single stage proposed 4-phase charge pump with CWPM in "Balios".

| Device | Type | Channel Width ($\mu m$) | Channel Length ($\mu m$) | Capacitor Value ($pF$) |
|---|---|---|---|---|
| M1 | NMOSIM | 24 | 0.5 | - |
| M2 | NMOSIM | 24 | 0.5 | - |
| M3 | PMOSIM | 36 | 0.5 | - |
| M4 | PMOSIM | 36 | 0.5 | - |
| M5 | NMOSIM | 1 | 0.5 | - |
| M6 | NMOSIM | 1 | 0.5 | - |
| M7 | PMOSIM | 3 | 0.5 | - |
| M8 | PMOSIM | 3 | 0.5 | - |
| M9 | PMOSIM | 3 | 0.5 | - |
| M10 | PMOSIM | 3 | 0.5 | - |
| C1 | CPM | - | - | 5.193 |
| C2 | CPM | - | - | 5.193 |
| C3 | CPM | - | - | 0.216 |
| C4 | CPM | - | - | 0.216 |

**Table B.2.:** Device parameters of a single stage proposed 4-phase charge pump with CPM in "Balios".

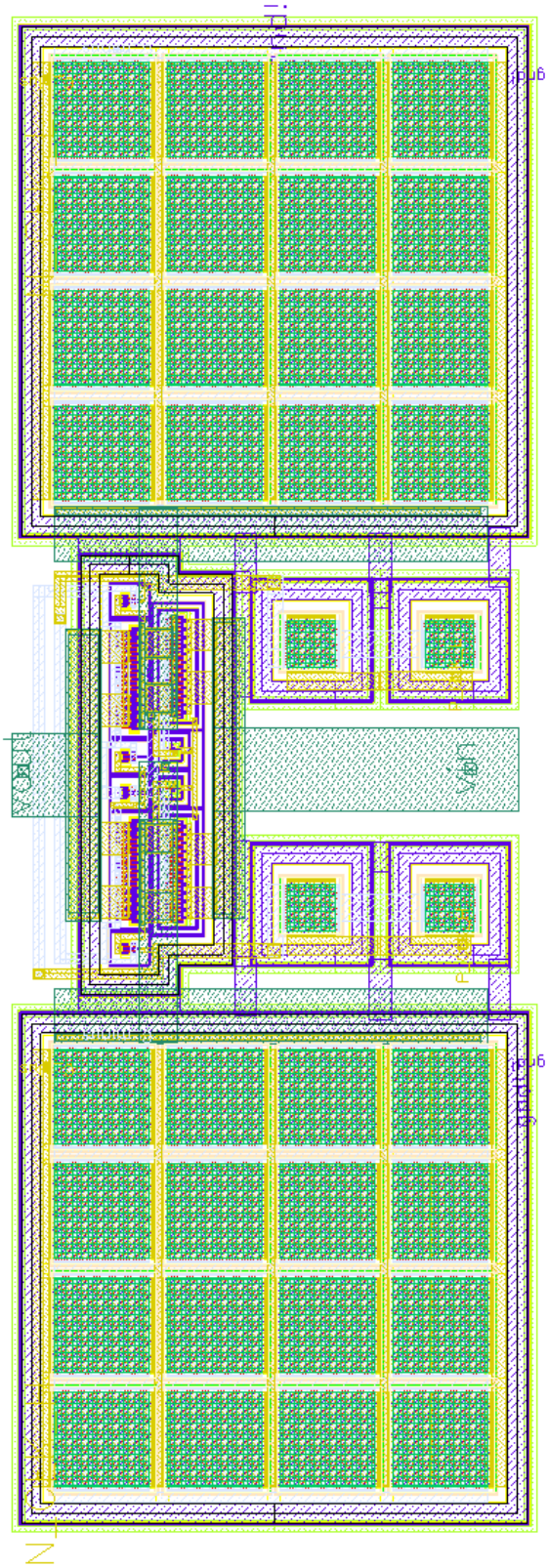

**Figure B.1.:** Layout of a single stage proposed 4-phase charge pump with CWPM in "Balios".

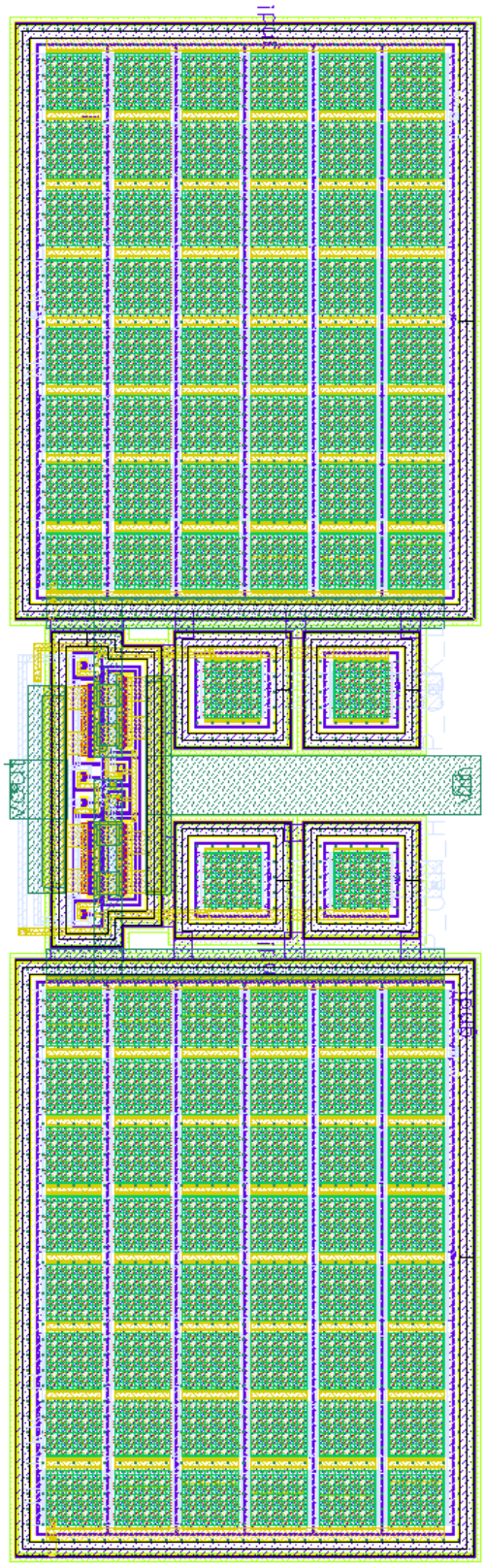

**Figure B.2.:** Layout of a single stage proposed 4-phase charge pump with CPM in "Balios".

# C VHDL Code for the Generation of Proposed 4-phase Clock Schemes in FPGA

**VHDL code for one channel clock generation:**

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    18:59:19 12/17/2012
-- Design Name:
-- Module Name:    generator - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use IEEE.std_logic_arith.all;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;



entity generator is

        port (
                High_puls_width: in integer range 255 downto 0 ;
```

```
                Low_puls_width: in integer range 255 downto 0 ;
                Delay_width: in integer range 255 downto 0 ;
                clk : in std_logic ;
                reset: in std_logic ;
                output  : out std_logic
        );
end generator;

architecture synth of generator is

type FSM is (delays,high,low); -- Finte State Machine
signal CURR_STATE,NEXT_STATE: FSM;
signal timer_delay,timer_High,timer_Low : std_logic;
-- 3 signal to indecate the end of the count of each counter
signal Counter_H,Counter_D,Counter_L: integer range 255 downto 0:=0;
-- 3 counter
signal next_Counter_D,next_Counter_H,next_Counter_L: integer
range 255 downto 0:=0;
begin

SYNC: process (CLK,reset)
begin
                if reset = '1' then
                        CURR_STATE <= delays;
                        Counter_D<=0;
                        Counter_H<=1;
                        Counter_L<=1;
                elsif rising_edge (CLK) then

                        CURR_STATE <= NEXT_STATE;
                        Counter_D<=next_Counter_D;
                        Counter_H<=next_Counter_H;
                        Counter_L<= next_Counter_L ;
                end if;
end process SYNC;

STATE_MACHINE: process (CURR_STATE,Counter_D,Counter_H,Counter_L,
High_puls_width,Low_puls_width,Delay_width)
begin
                -- Hold Value
         next_Counter_D    <= Counter_D;
         next_Counter_H <=Counter_H;
         next_Counter_L <=Counter_L;
    timer_delay   <= '0';
    timer_High <= '0';
    timer_Low <= '0';
        case (CURR_STATE) is
                when delays =>
        next_Counter_D <= Counter_D + 1;
        if (Counter_D = Delay_width ) then
```

```
          next_Counter_D  <= 0;
          timer_delay  <= '1';
        end if;
                when high =>
         next_Counter_H <= Counter_H + 1;
        if (Counter_H = High_puls_width) then
          next_Counter_H  <= 1;
          timer_High  <= '1';
        end if;
                when low =>
        next_Counter_L <= Counter_L + 1;
        if (Counter_L = Low_puls_width) then
          next_Counter_L  <= 1;
          timer_Low  <= '1';
        end if;
                when others =>
 end case;
end process STATE_MACHINE;

sm :process (CURR_STATE,timer_delay,timer_High,timer_Low)
begin
NEXT_STATE<=CURR_STATE;
case(CURR_STATE)is
 when delays =>
        if timer_delay='1' then
         NEXT_STATE<= high;
        end if;
 when high =>
        if timer_High='1' then
         NEXT_STATE<= low;
        end if;
 when low =>
        if timer_Low='1' then
         NEXT_STATE<= high;
        end if;
 when others =>
end case;
end process sm;

oo :process (CURR_STATE)
begin
case(CURR_STATE)is
 when delays =>
        output <= '0';
 when high =>
        output <= '1';
 when low =>
        output <= '0';
 when others =>
end case;
```

```
end process oo;

end synth;
```

**VHDL code for 4 channel clock generation:**

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    11:36:57 01/07/2013
-- Design Name:
-- Module Name:    generator_4_phase - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;
use work.all;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity generator_4_phase is
    Port (

                        clk_IN1_P : in std_logic;
                        clk_IN1_N : in std_logic;
                        reset : in  STD_LOGIC;
                        clk_out : out  STD_LOGIC_VECTOR (3 downto 0)

          );
end generator_4_phase;
```

```
architecture Behavioral of generator_4_phase is
signal clk : std_logic ;
component generator
        port (
                High_puls_width: in integer range 255 downto 0;
                Low_puls_width: in integer range 255 downto 0;
                delay_width: in integer range 255 downto 0;
                clk : in std_logic ;
                reset: in std_logic ;
                output  : out std_logic
        );
end component;

component clock
port
 (-- Clock in ports
  CLK_IN1_P         : in     std_logic;
  CLK_IN1_N         : in     std_logic;
  -- Clock out ports
  CLK_OUT1          : out    std_logic;
  -- Status and control signals
  RESET             : in     std_logic
 );
end component;
begin
-- MMCM to increase the input frequency
MMCM : clock
   port map
    (-- Clock in ports
     CLK_IN1_P => CLK_IN1_P,
     CLK_IN1_N => CLK_IN1_N,
     -- Clock out ports
     CLK_OUT1 => CLK,
     -- Status and control signals
     RESET  => RESET);
-- Chanel parameters can be changed     here
Kanal_0: generator
        port map(
                High_puls_width=> 17,
                Low_puls_width => 17,
                delay_width => 0,
                clk => clk,
                reset => reset,
                output  => clk_out(0)
        );

Kanal_1: generator
        port map(
                High_puls_width=> 17,
                Low_puls_width => 17,
```

```
                delay_width => 1,
                clk => clk,
                reset => reset,
                output  => clk_out(1)
        );
Kanal_2: generator
        port map(
                High_puls_width=> 14,
                Low_puls_width => 20,
                delay_width => 17,
                clk => clk,
                reset => reset,
                output  => clk_out(2)
        );
Kanal_3: generator
        port map(
                High_puls_width=> 18,
                Low_puls_width => 16,
                delay_width => 0,
                clk => clk,
                reset => reset,
                output  => clk_out(3)
        );


end Behavioral;\\
```

**ucf-file for the 4-phase clock generator in the Virtex-6 FPGA ML605 evaluation kit:**

```
CONFIG PART = xc6vlx240tff1156-1;

########## ML605 Board ##########
NET "CLK_IN1_P" IOSTANDARD = LVDS_25;
NET "CLK_IN1_P" DIFF_TERM = "TRUE";
NET "CLK_IN1_P" SLEW = FAST;
NET "CLK_IN1_P" LOC = J9;
NET "clk_IN1_N" IOSTANDARD = LVDS_25;
NET "clk_IN1_N" DIFF_TERM = "TRUE";
NET "clk_IN1_N" SLEW = FAST;
NET "clk_IN1_N" LOC = H9;
NET "CLK_IN1_P" TNM_NET = "CLK_IN1_P";
TIMESPEC TS_CLK_IN1_P = PERIOD "CLK_IN1_P" 5 ns HIGH 50
% INPUT_JITTER 50 ps;

NET "reset" TIG;
NET "reset" IOSTANDARD = LVCMOS15;
NET "reset" LOC = G26;

# downgrade the Place:1153 error in the mapper
NET "reset" CLOCK_DEDICATED_ROUTE = FALSE;
```

```
# PlanAhead Generated physical constraints

NET "clk_out[0]" LOC = AC22 | IOSTANDARD = LVCMOS25 | slew = FAST;
NET "clk_out[1]" LOC = AC24 | IOSTANDARD = LVCMOS25 | slew = FAST;
NET "clk_out[2]" LOC = AE22 | IOSTANDARD = LVCMOS25 | slew = FAST;
NET "clk_out[3]" LOC = AE23 | IOSTANDARD = LVCMOS25 | slew = FAST;
```

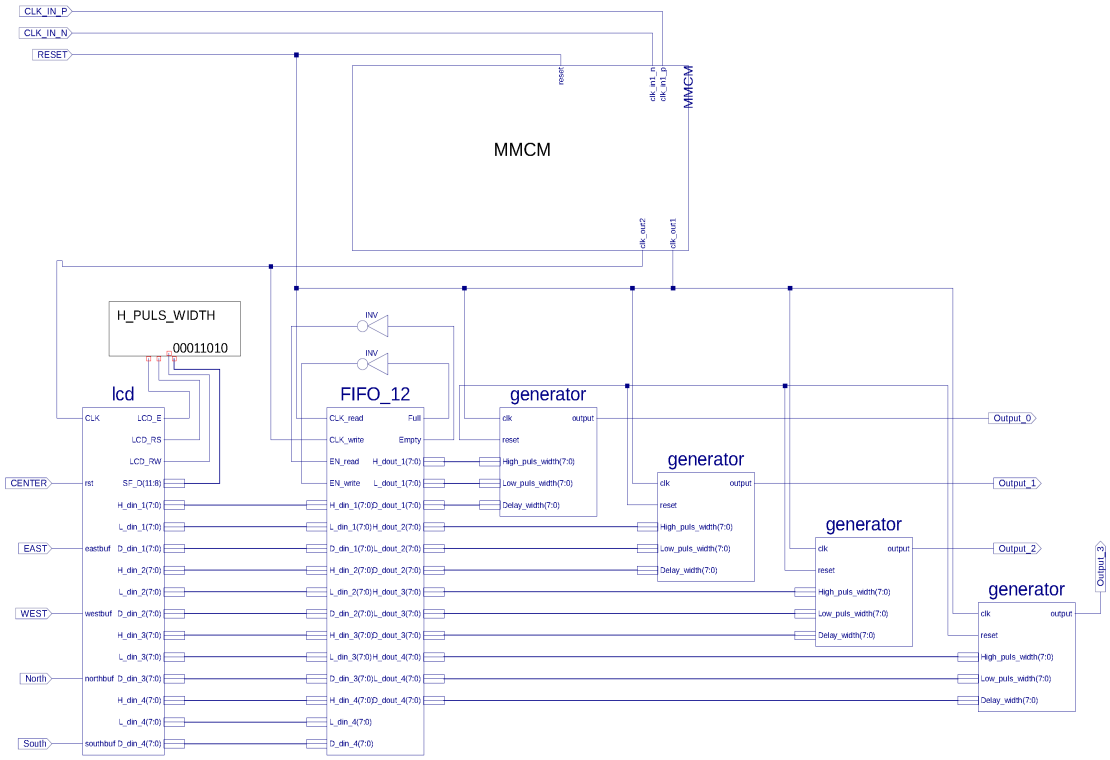


**Figure C.1.:** Block diagram of the 4-phase clock generator in FPGA.

# D IC Package and Pin List of "Balios"

| Direction | Type | Pin Nr. | Signal Name |
|---|---|---|---|
| out | analog | 47 | Vout, high voltage output up to 120 $V$ |
| in | analog | 72 | V_cp, DC power supply for the charge pump |
| in | analog | 73 | V_cp, DC power supply for the charge pump |
| inout | analog | 74 | V_gnd, ground for the charge pump |
| in | analog | 75 | Vsupply_4phase, DC power supply for the clock generator |
| out | analog | 76 | Vsupply_4phase_extra, DC power supply for the separate clock generator |
| in | digital | 77 | osc_clk_plus_ext, external 2-phase clock signal (plus) for the clock generator |
| in | digital | 78 | sel_osc, enable signal for external 2-phase clock signals at the clock generator |
| in | digital | 79 | osc_clk_min_ext, external 2-phase clock signal (minus) for the clock generator |
| in | digital | 80 | sel_4phase, enable signal for external 4-phase clock signals at the clock generator |
| out | digital | 81 | clk_plus_out, clock signal (plus) of the separate clock generator |
| out | digital | 82 | clk_min_out, clock signal (minus) of the separate clock generator |
| out | digital | 83 | takt_d_extra, clock signal D of the separate clock generator |
| out | digital | 84 | takt_c_extra, clock signal C of the separate clock generator |
| out | digital | 1 | takt_b_extra, clock signal B of the separate clock generator |
| out | digital | 2 | takt_a_extra, clock signal A of the separate clock generator |
| in | digital | 3 | clkD_ext, external 4-phase clock D signal for the clock generator |
| in | digital | 4 | clkC_ext, external 4-phase clock C signal for the clock generator |
| in | digital | 5 | clkB_ext, external 4-phase clock B signal for the clock generator |
| in | digital | 6 | clkA_ext, external 4-phase clock A signal for the clock generator |
| inout | analog | 7 | V_gnd, ground for the clock generator (charge pump) |
| inout | analog | 8 | V_gnd, ground for the separate clock generator (charge pump) |
| in | analog | 9 | Vin, input of the charge pump |
| inout | analog | 10 | V_gnd, ground for the charge pump |
| in | analog | 11 | V_cp, DC power supply for the charge pump |
| in | analog | 12 | V_cp, DC power supply for the charge pump |

**Table D.1.:** Pin list of "Balios" in JLCC84.

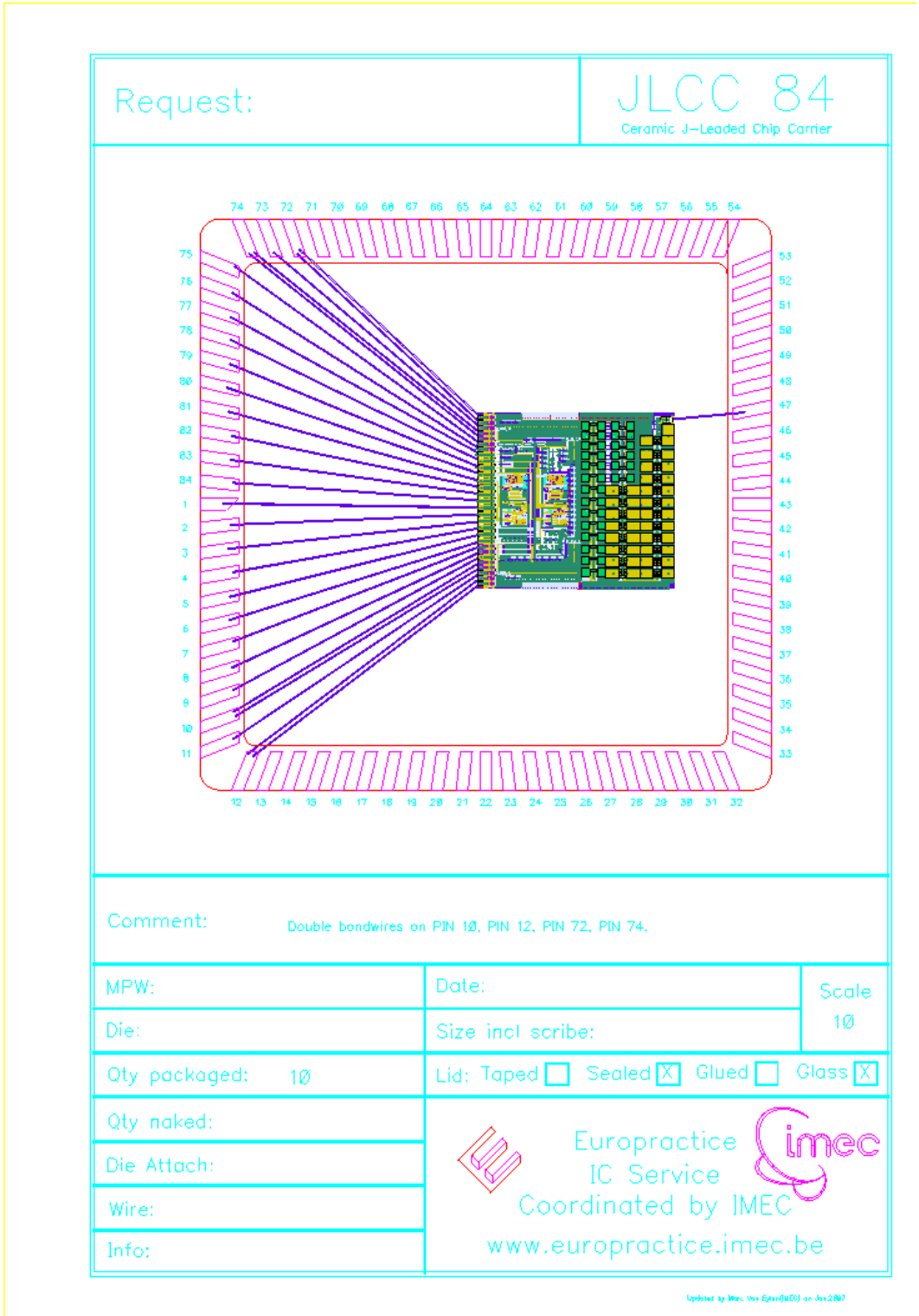


**Figure D.1.:** Bonding plan of "Balios" using package JLCC84.

# E Evaluation Board for "Balios"

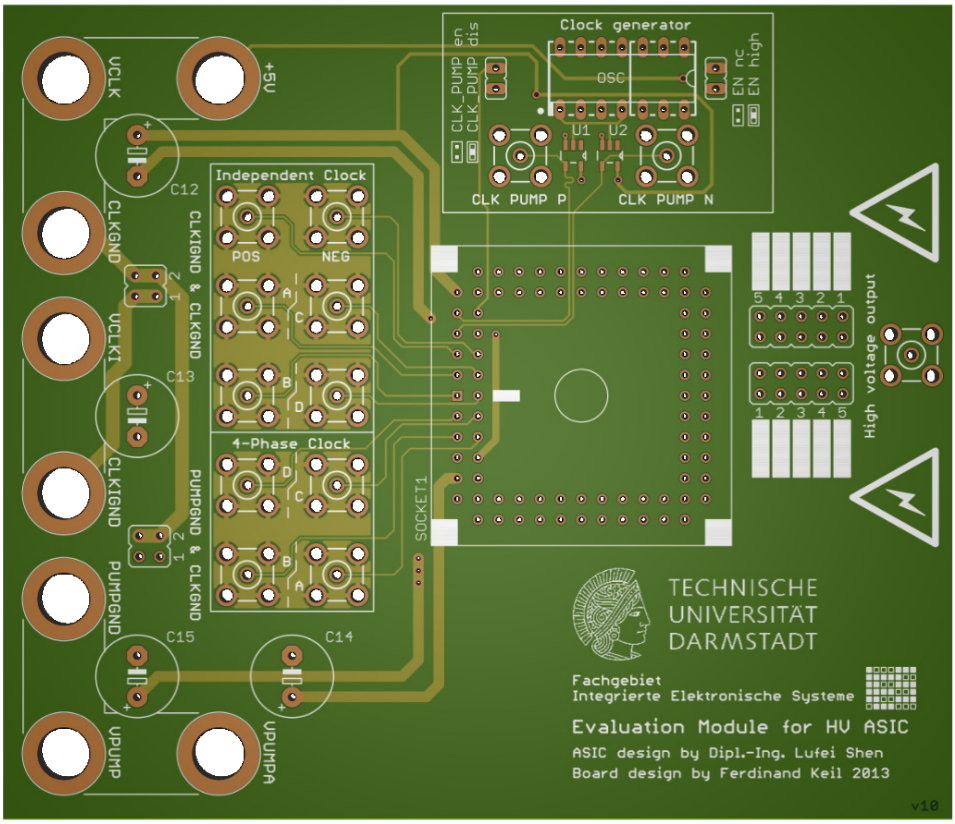


**Figure E.1.:** Top view of the evaluation board for "Balios".

**Remarks:** One enable signal for the external 4-phase clock signals at Pin 80 of JLCC84 is missing on the evaluation board. It can be accessed through the package JLCC84 from the bottom side of the evaluation board. The ClkD and ClkA of the independent clock generator should change their places with each other.

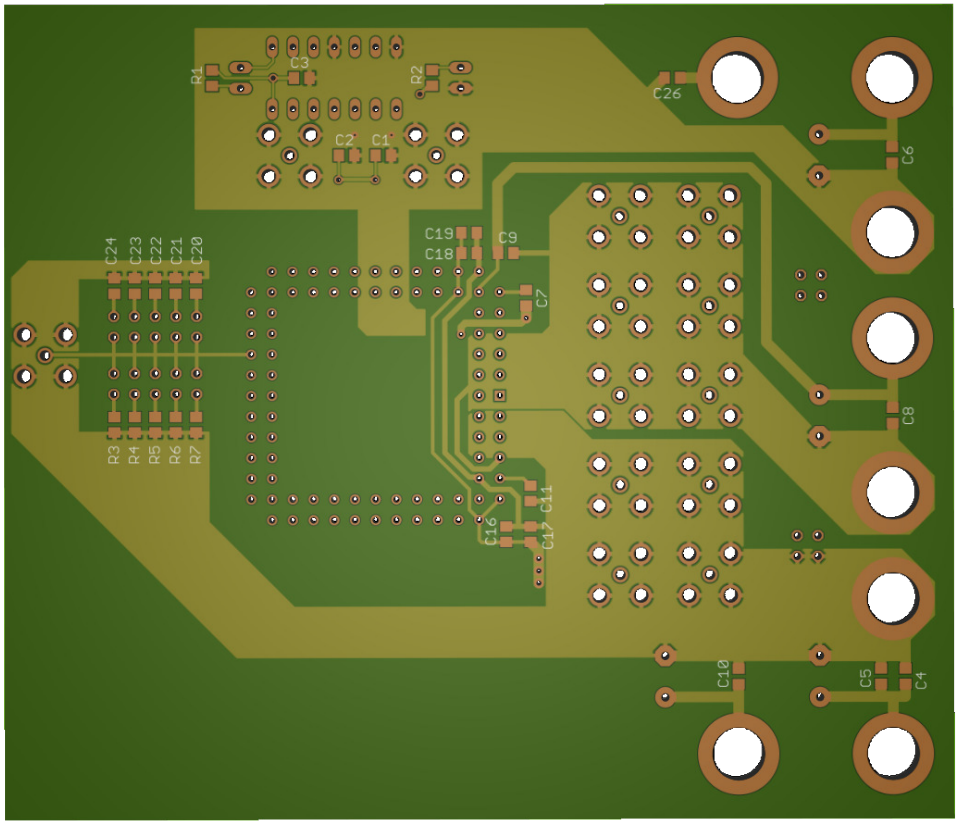


**Figure E.2.:** Bottom view of the evaluation board for "Balios".

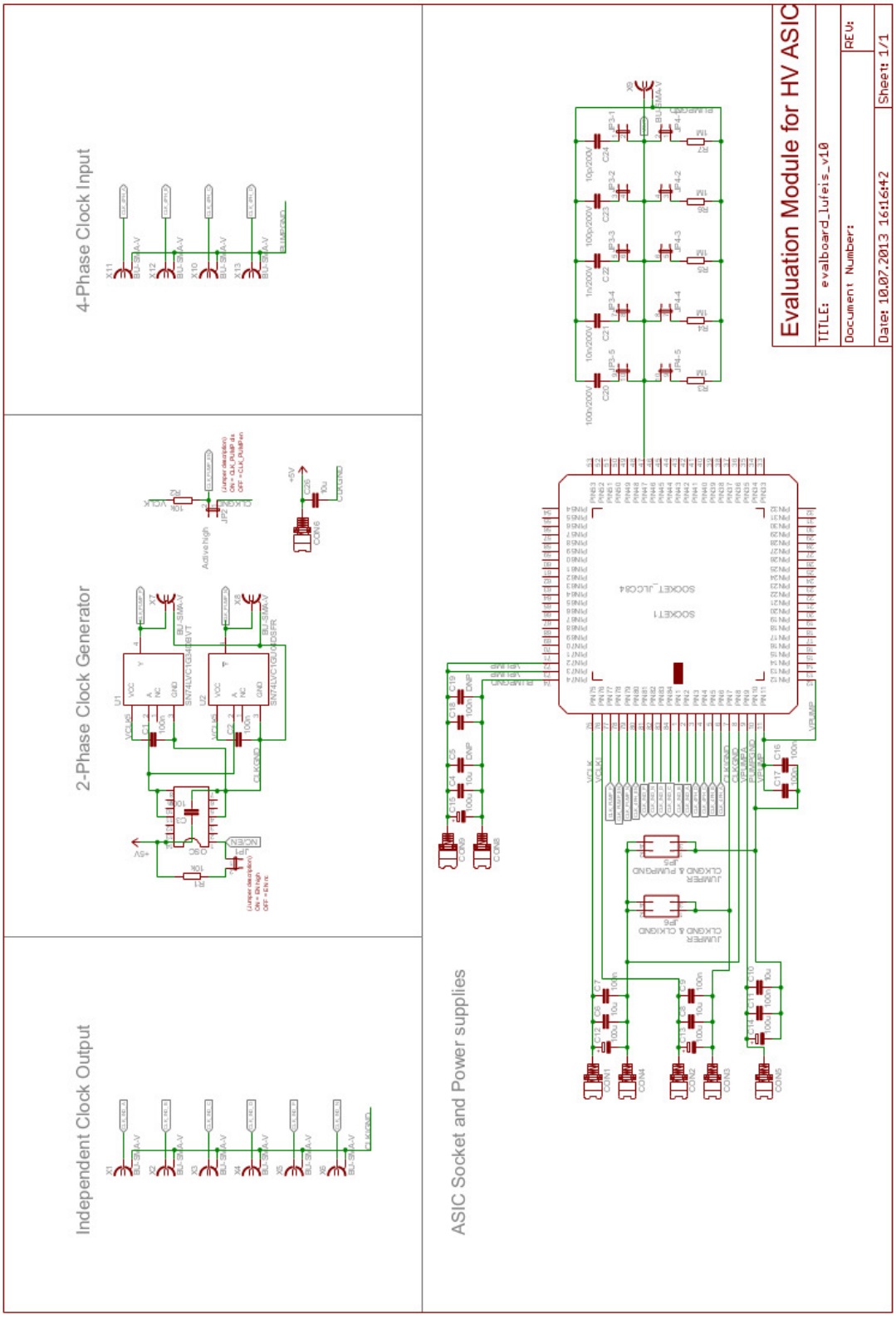


**Figure E.3.:** Schematic circuit of the evaluation board for "Balios".

| RefDes | Value | Device | Package | Company |
|---|---|---|---|---|
| C1,C2, | 100 $nF$ | 2C-EUC0805 | C0805 | - |
| C3,C7,C9 | 100 $nF$ | 2C-EUC0805 | C0805 | - |
| C11,C16 | 100 $nF$ | 2C-EUC0805 | C0805 | - |
| C17,C18 | 100 $nF$ | 2C-EUC0805 | C0805 | - |
| C4,C6,C8 | 10 $\mu F$ | C-EUC0805 | C0805 | Murata |
| C10,C26 | 10 $\mu F$ | C-EUC0805 | C0805 | Murata |
| C5,C19 | DNP | C-EUC0805 | C0805 | - |
| C12,C13 | 100 $\mu F$ | CPOL-EUE5-10.5 | E5-10,5 | Panasonic |
| C14,C15 | 100 $\mu F$ | CPOL-EUE5-10.5 | E5-10,5 | Panasonic |
| C20 | 100 $nF$ (200 $V$) | C-EUC0805 | C0805 | TDK |
| C21 | 10 $nF$ (200 $V$) | C-EUC0805 | C0805 | Murata |
| C22 | 1 $nF$ (200 $V$) | C-EUC0805 | C0805 | Murata |
| C23 | 100 $pF$ (200 $V$) | C-EUC0805 | C0805 | Kemet |
| C24 | 10 $pF$ (200 $V$) | C-EUC0805 | C0805 | Kemet |
| CON1,CON2 | BANANA JACK 4MM | BANANA JACK 4MM | 4MM BANANA JACK | - |
| CON3,CON4 | BANANA JACK 4MM | BANANA JACK 4MM | 4MM BANANA JACK | - |
| CON5,CON6 | BANANA JACK 4MM | BANANA JACK 4MM | 4MM BANANA JACK | - |
| CON8,CON9 | BANANA JACK 4MM | BANANA JACK 4MM | 4MM BANANA JACK | - |
| JP1,JP2 | JP1E | JP1 | jumper | - |
| JP3,JP4 | JP5QE | JP5Q | jumper | - |
| JP5,JP6 | JP2Q | JP2Q | jumper | - |
| OSC | DIL14 | DIL14 | ic-package | - |
| R1,R2 | 10 $k\Omega$ | R-EU R0805 | R0805 | - |
| R3,R4, | 1 $M\Omega$ | R-EU R0805 | R0805 | Yageo |
| R5,R6,R7 | 1 $M\Omega$ | R-EU R0805 | R0805 | Yageo |
| SOCKET1 | SOCKET JLCC84 | SOCKET JLCC84 | TEXTOOL JLCC84 | - |
| U1 | SN74LVC 1G34DBVT | SN74LVC1G34DBVT | SOT95P280X145-5N | Texas Instruments |
| U2 | SN74LVC 1GU04DSFR | SN74LVC1GU04DSFR | SOT95P280X145-5N | Texas Instruments |
| X1,X2,X3 | BU-SMA-V | BU-SMA-V | BU-SMA-V | LPRS |
| X4,X5,X6,X7 | BU-SMA-V | BU-SMA-V | BU-SMA-V | LPRS |
| X8,X9,X10 | BU-SMA-V | BU-SMA-V | BU-SMA-V | LPRS |
| X11,X12,X13 | BU-SMA-V | BU-SMA-V | BU-SMA-V | LPRS |

**Table E.1.:** Component list of the evaluation board for "Balios".

# F Design Flow for High Voltage CMOS ASICs Proposed by AMS

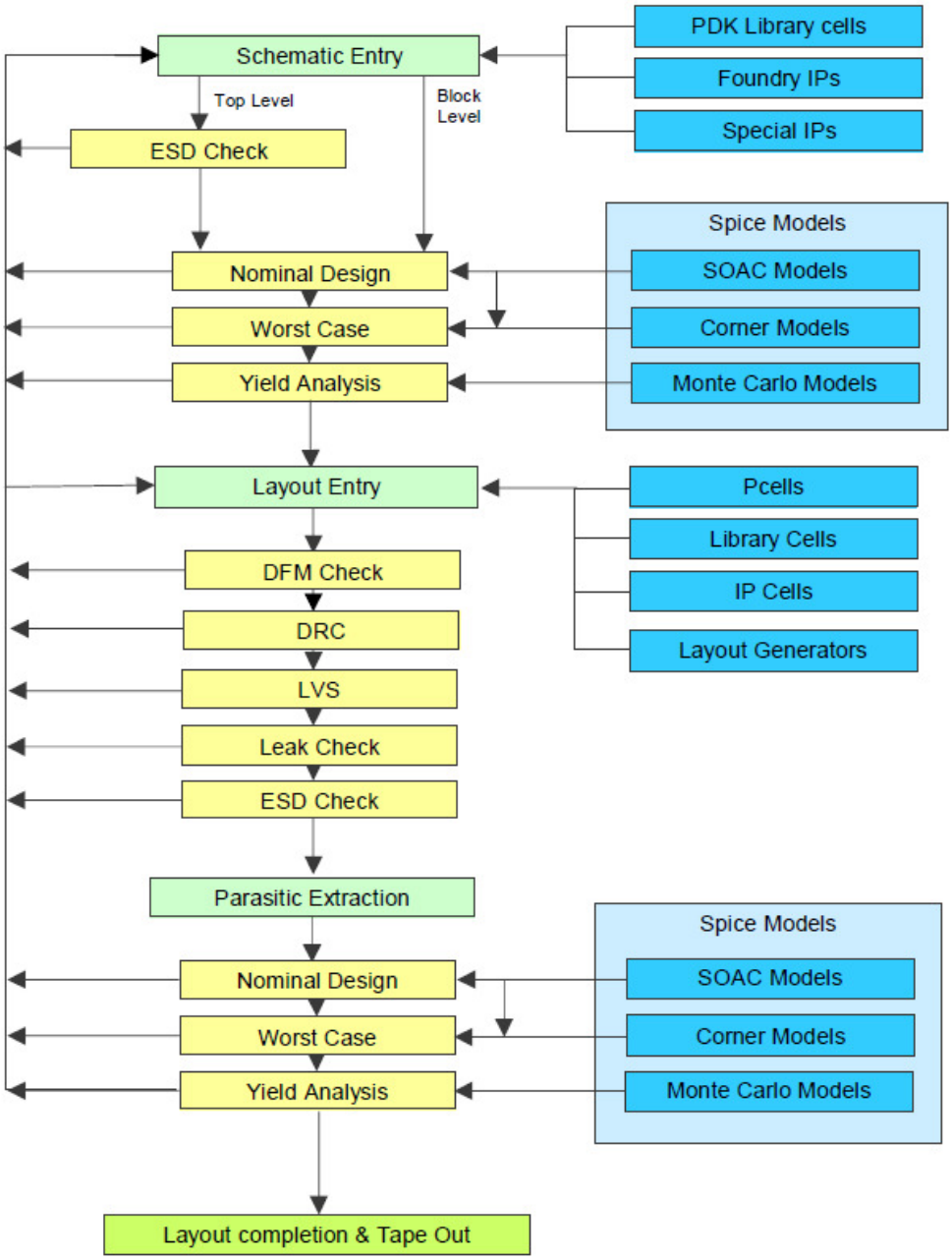


**Figure F.1.:** Design flow for high voltage CMOS ASICs proposed by AMS [Doc14d].

# Curriculum Vitae

## Personal Data

| | |
|---|---|
| Name | Lufei Shen |
| Gender | Male |
| Date of birth | 30. July 1982 |
| Place of birth | Fengjing, Shanghai, China |

## Education

| | |
|---|---|
| 09/1989–07/1995 | Fengjing Elementary School, Shanghai, China |
| 09/1995–07/1998 | Fengjing Middle School, Shanghai, China |
| 09/1998–07/2001 | Jinshan High School, Shanghai, China |
| 09/2001–07/2006 | Bachelor of Science (B.Sc.) in Electrical Engineering, focus "Electronic Information Engineering" (Tongji University, Shanghai, China) |
| 10/2006–10/2009 | Diploma (Dipl.-Ing.) in Electrical Engineering, focus "Microelectronics" (Technische Universität Darmstadt, Germany) |

## Work Experience

| | |
|---|---|
| 10/2008–02/2009 | Internship at the Department Smart Power Technology Development, Infineon Technologies AG, Regensburg, Germany |
| 01/2010–12/2014 | Research and Teaching Staff, *Integrated Electronic Systems Lab*, Technische Universität Darmstadt, Germany |